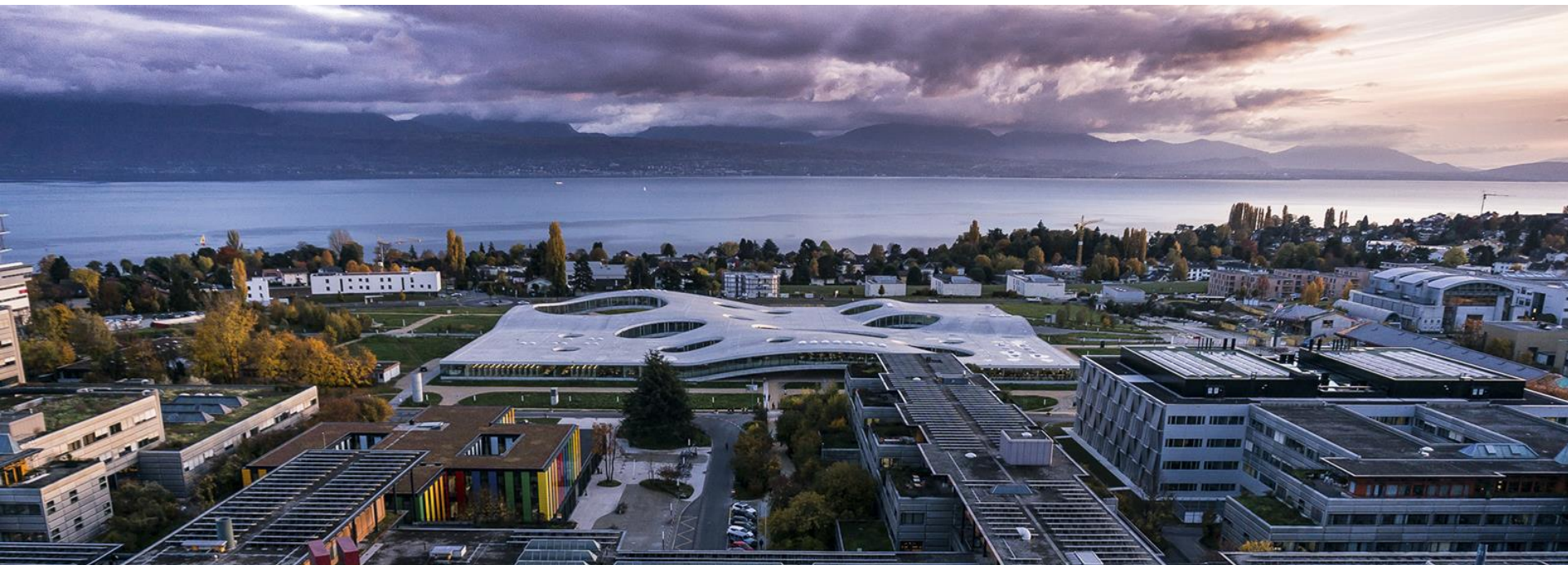




GaN electronic devices

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Power and Wide-band-gap Electronics Research (POWERlab)

Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

Lecture I: Electronic devices

- Introduction
- Heterostructures
- Lateral devices: HEMTs

Lecture II: Lateral Power devices

- E- and D-mode devices
- Reaching low resistance and high voltage
- current commercial technology
- Losses in GaNpower devices

Lecture III: Vertical Power devices

- Introduction
- Vertical devices: GaN PN diodes and MOSFETs
- Novel concepts in vertical power electronics

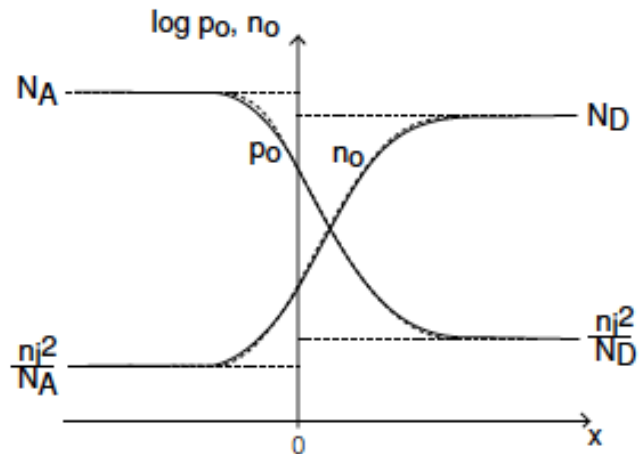
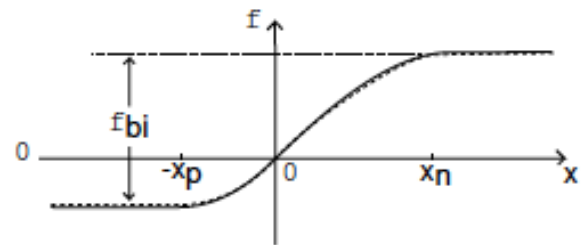
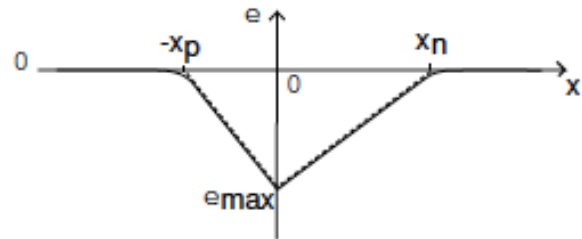
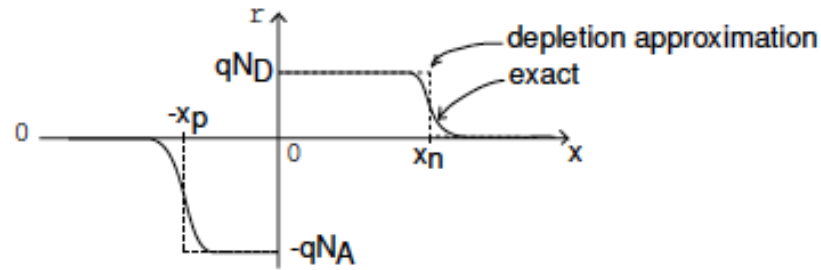
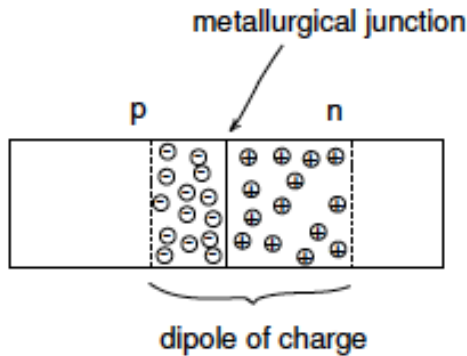
Lecture IV: RF devices

- Equivalent circuit and FOM: important aspects
- Technologies to improve RF performance

Lecture V: Current trends – state of the art

- recent advances in the literature in GaN electronics
- superjunctions

Vertical GaN devices



Distinct regions:
Around metallurgical junction:
space charge region (SCR)

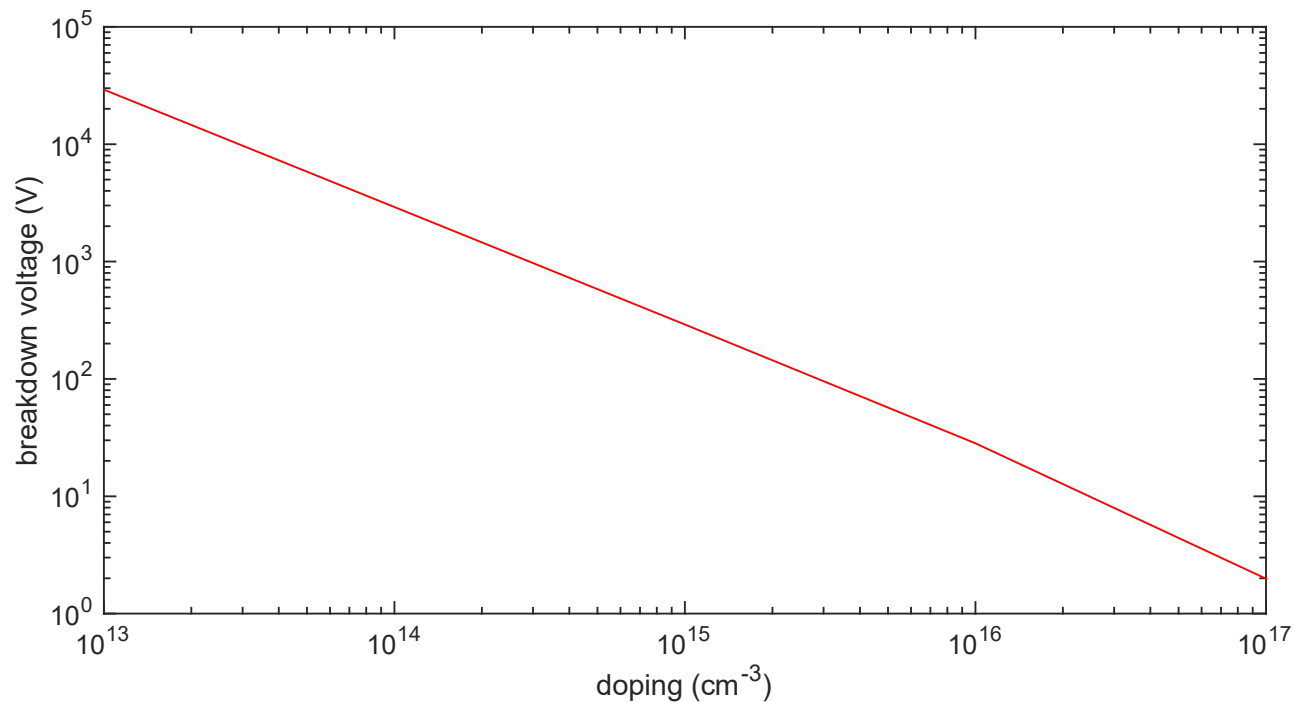
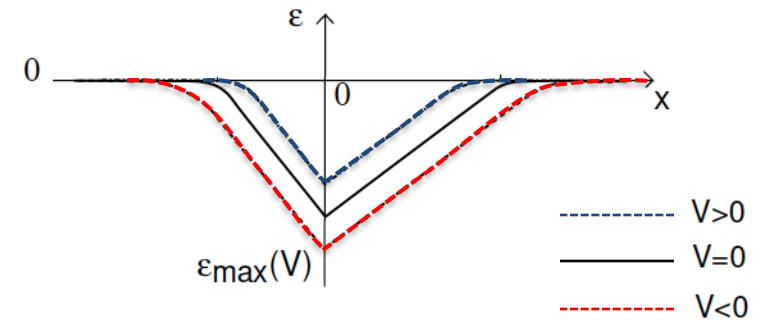
Far from junction:
quasi-neutral regions (QNR)
 $\rho \sim 0$

Electric field is constant and equal to zero

Ideal p-n junction out of equilibrium

Peak electric field:

$$|\mathcal{E}_{max}(V)| = \sqrt{\frac{2qN_A N_D (\phi_{bi} - V)}{\epsilon(N_D + N_A)}} = |\mathcal{E}_{max}(V=0)| \sqrt{1 - \frac{V}{\phi_{bi}}}$$



How to make a power device?

Power diodes

Goal:

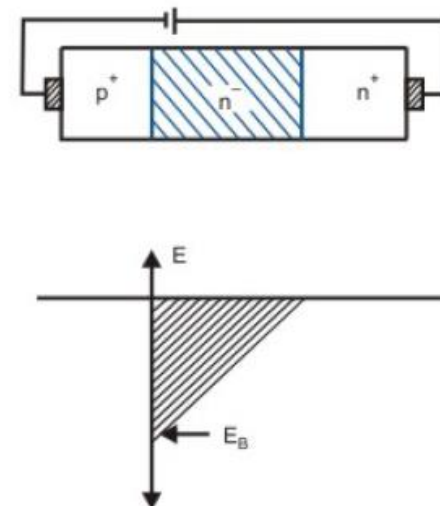
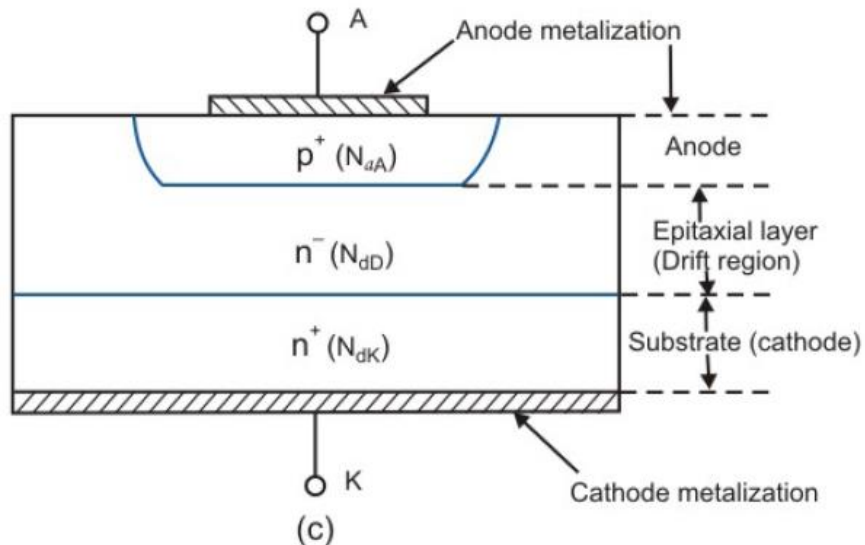
Conduct **several kilo amps** of current in the forward direction with very **little power loss** while blocking **several kilo volts** in the reverse direction.

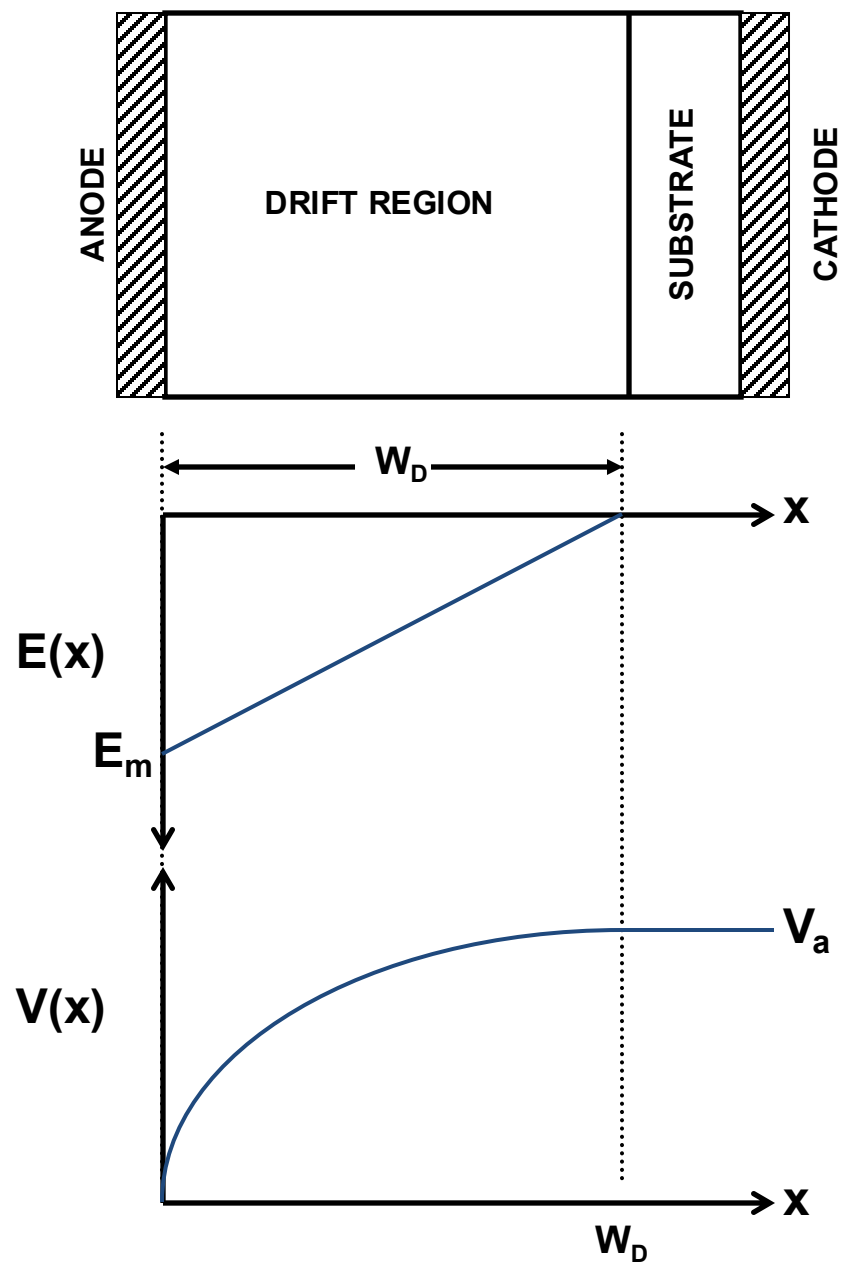
Large blocking voltage requires **wide depletion layer** in order to restrict the maximum electric field strength below the breakdown voltage (impact ionization level).

Space **charge density in the depletion layer should also be low** in order to yield a wide depletion layer for a given **maximum electric field strength**.

This is satisfied in a **lightly doped p-n junction diode of sufficient width** to accommodate the required depletion layer.

PIN diode





Ideal Specific On-Resistance ($R_{ON,SP}$):

$$W_D = \frac{2BV}{E_C} \quad \text{and} \quad N_D = \frac{\epsilon_s E_C^2}{2qBV}$$

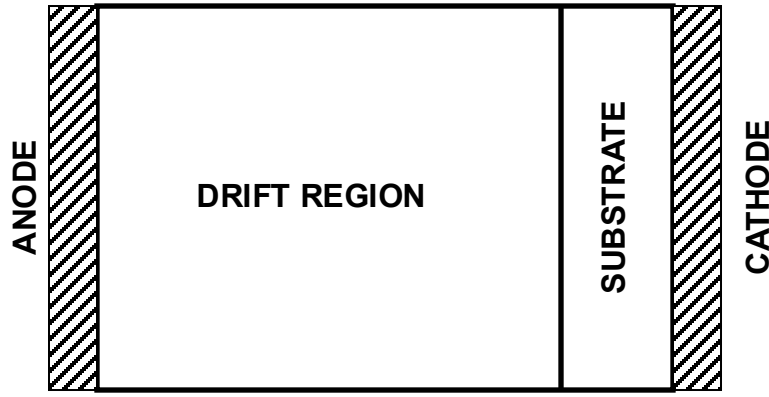
$$R_{ON,SP} = \frac{W_D}{q\mu_n N_D}$$

$$R_{ON,SP} = \frac{4BV^2}{\epsilon_s \mu_n E_C^3}$$

$R_{on,sp}$ is related to material properties

Baliga's figure of merit

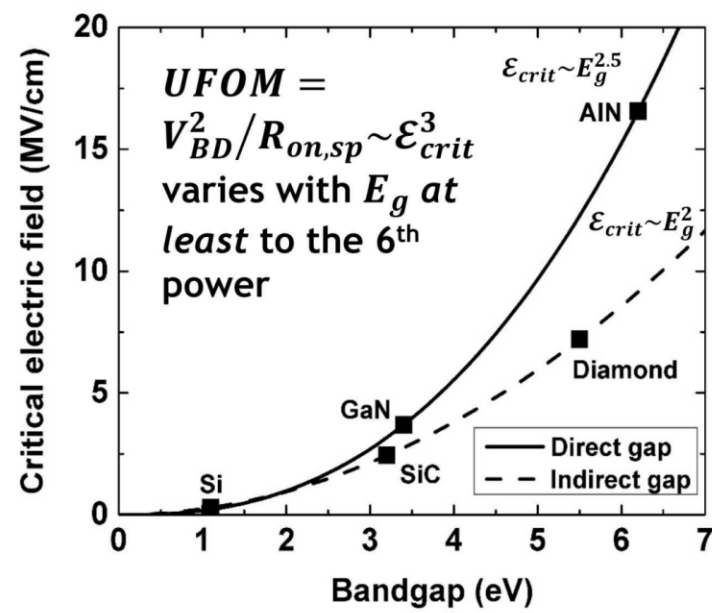
$$BFOM = \epsilon_s \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}$$



Baliga's figure of merit

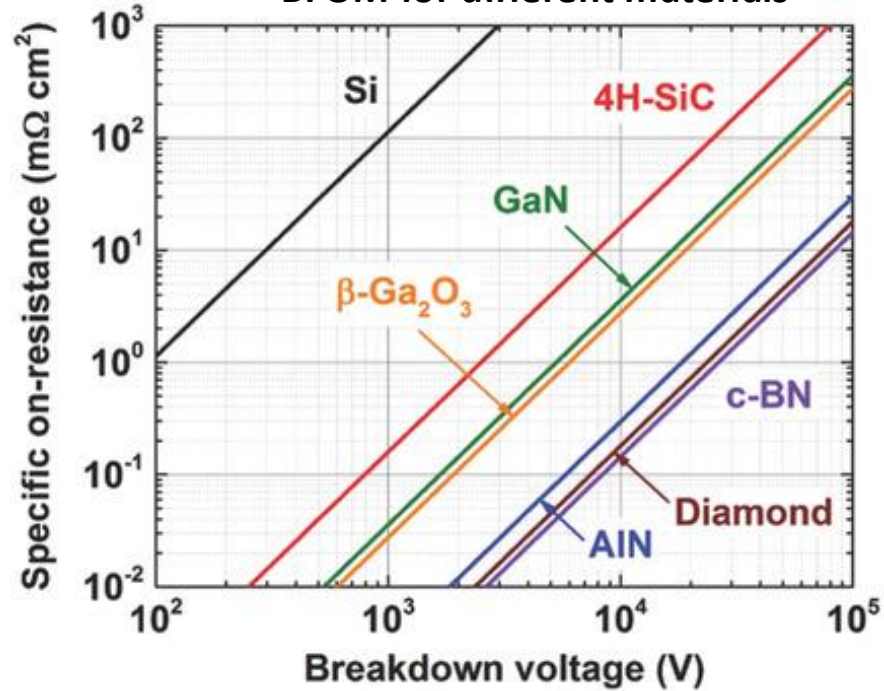
$$BFOM = \epsilon_s \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}$$

Relationship between Ec and Eg



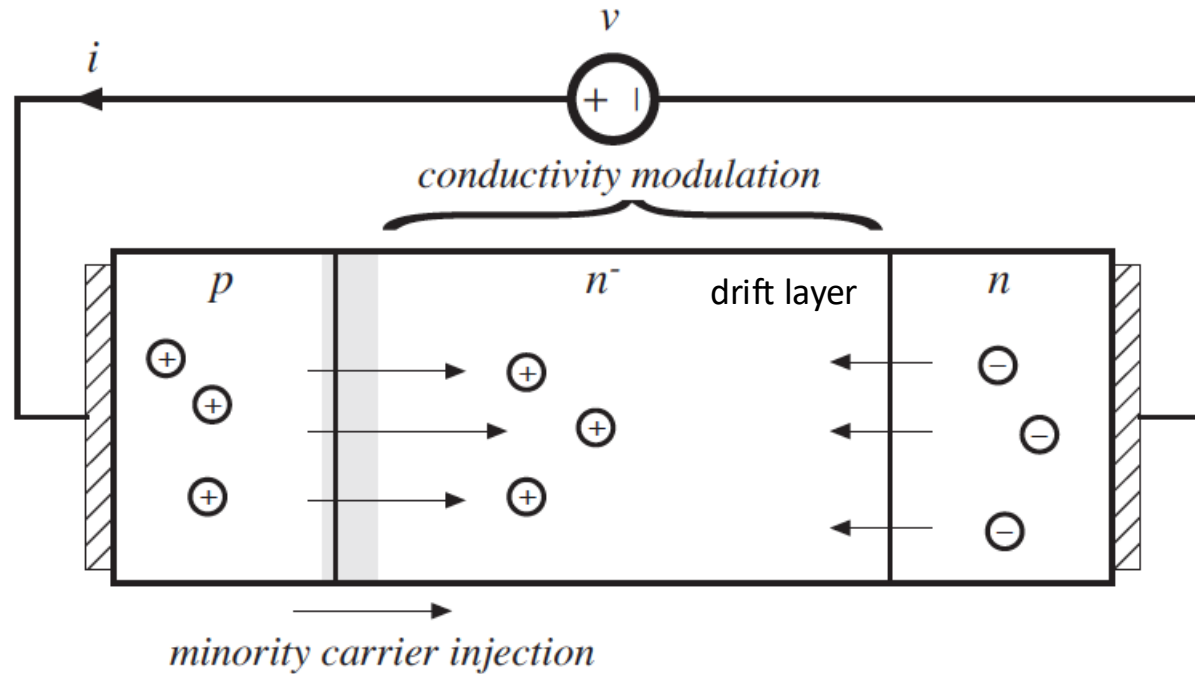
Hudgins et al., IEEE Trans. on Pow. Elec. 18, 3 (2003),
Tsao et al., Advanced Elec. Mat. 4, 1600501 (2018)

BFOM for different materials



diode PIN

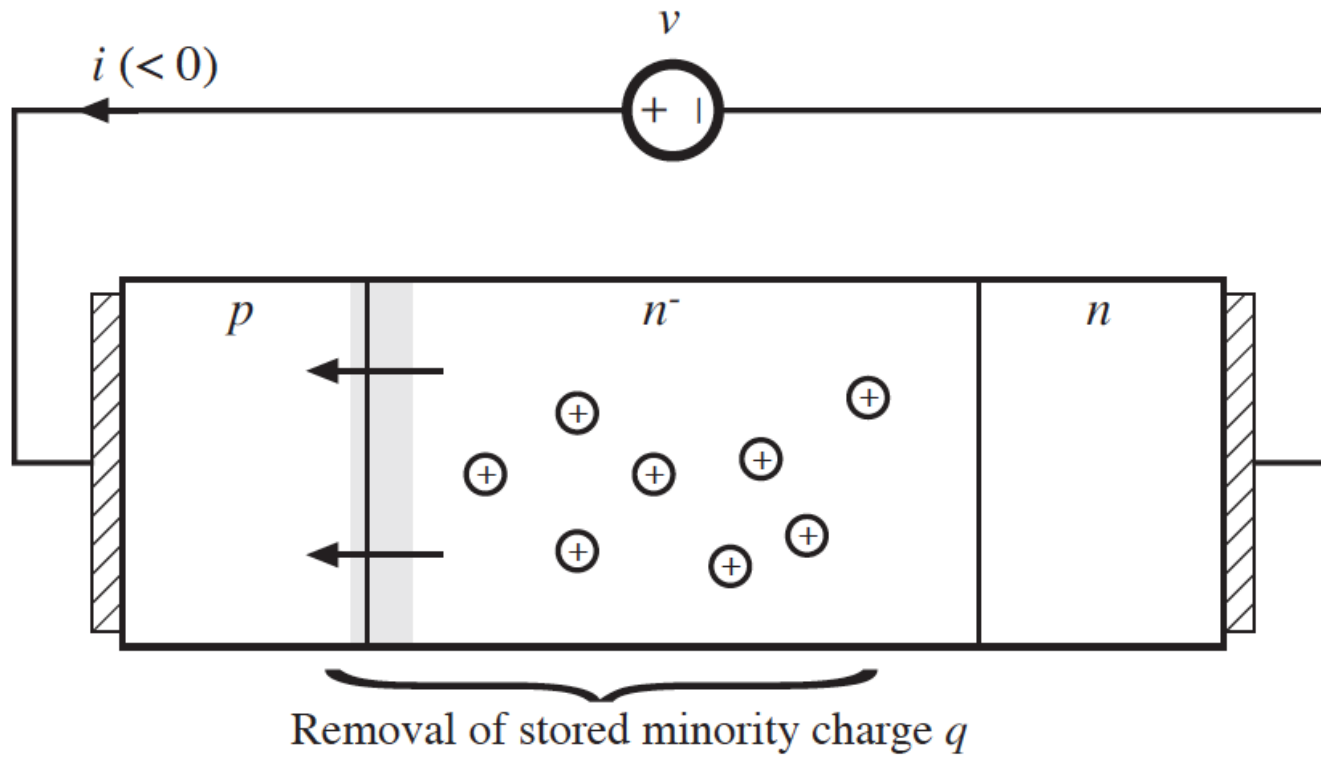
Forward polarization



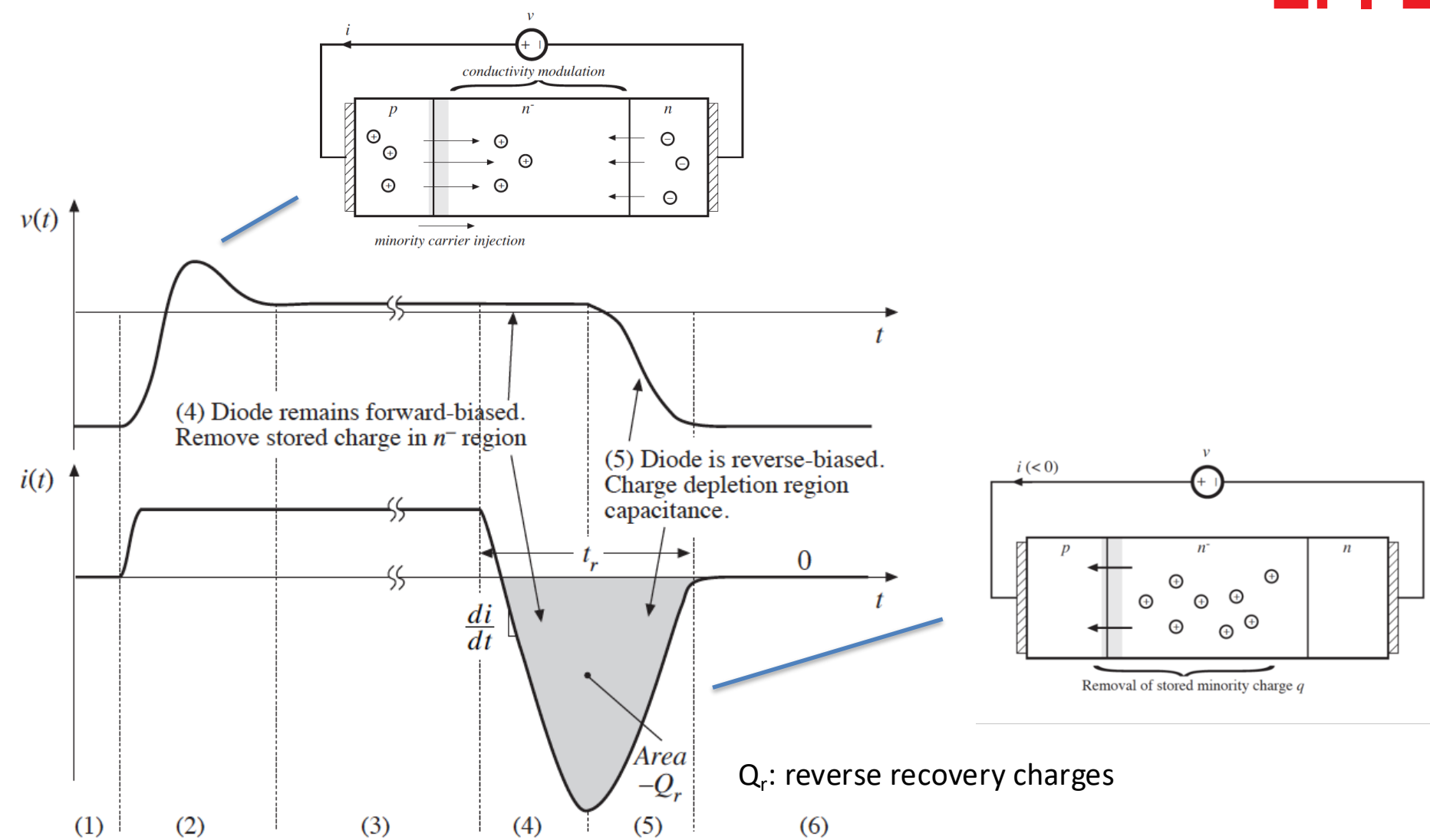
Forward polarization:

- Injection of minority carriers in the drift layer: conductivity modulation
- Charges are accumulated in the region «i»:
 - Resistance is reduced
 - But slows down the device
- Minority carrier device

Turn-off transient



Problem of PiN diodes



PiN diode is very slow! Not good for power converters!

However it is a great device structure to investigate the physics of materials

PIN diodes on bulk GaN

Pro:

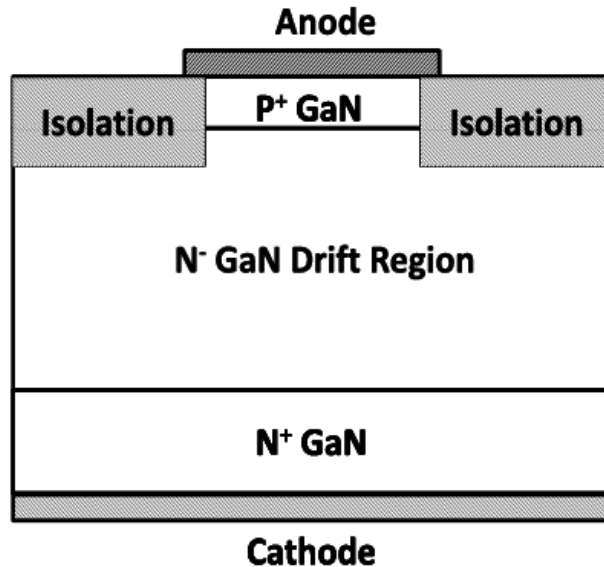
Bulk GaN eliminates lattice mismatch and allows growth of much thicker drift layers

Cons:

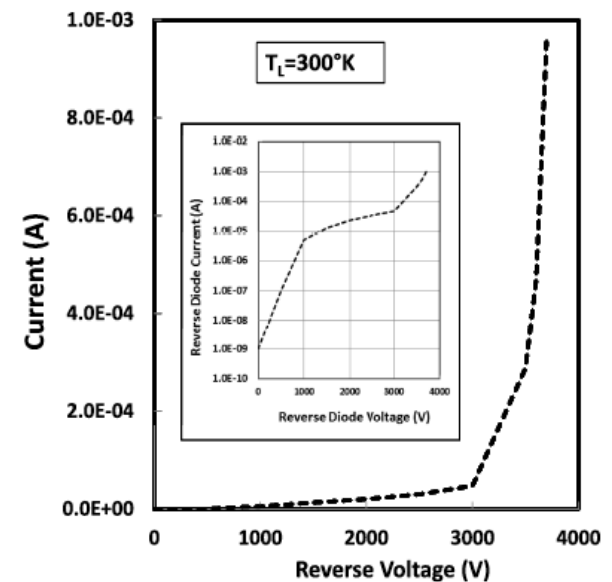
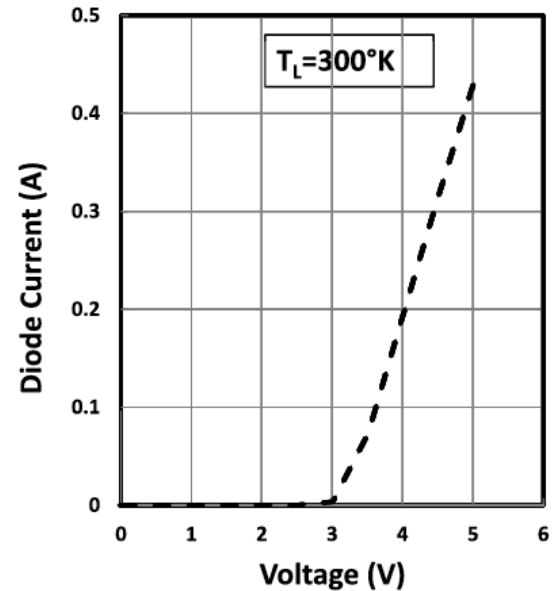
- Dislocation densities of 10^4 – 10^6 cm⁻², still much higher than those of Si and SiC substrates
- Small size (2–3 inch size) and relatively high cost (100 euro/cm²) of the GaN substrates, compared to 4–6 inch wafer size and reasonable cost (<10 \$/cm²) of SiC

GaN Power PIN diodes

PIN diodes on bulk GaN (30 μm drift layer)

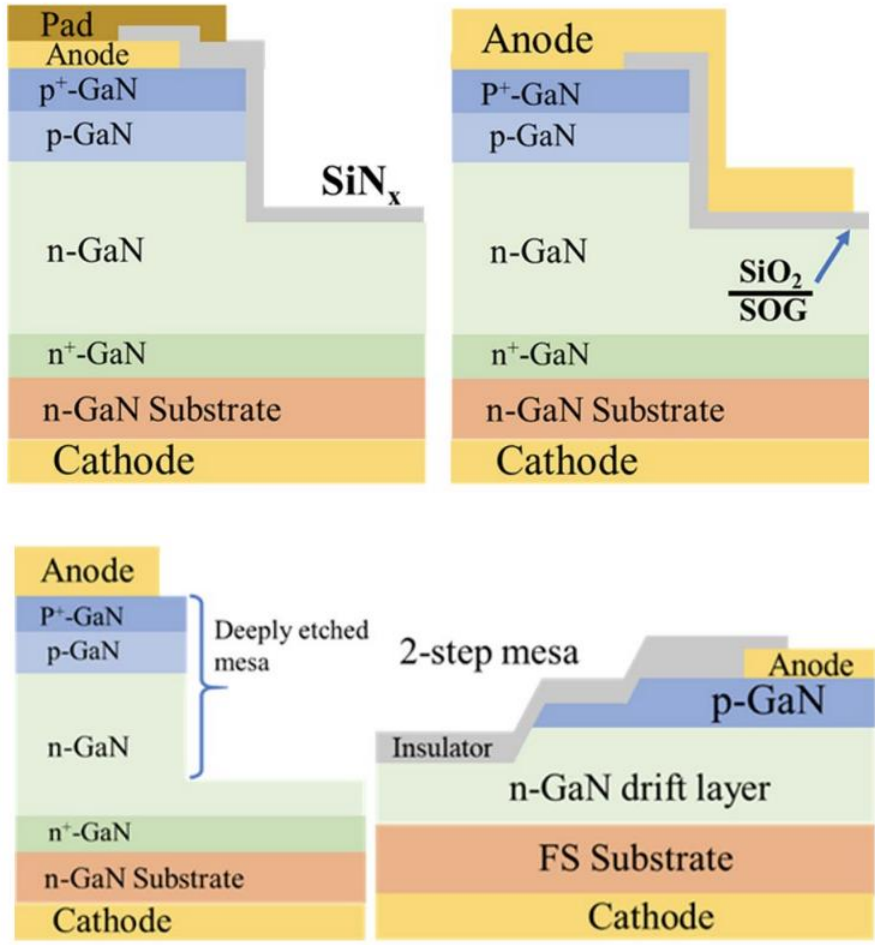
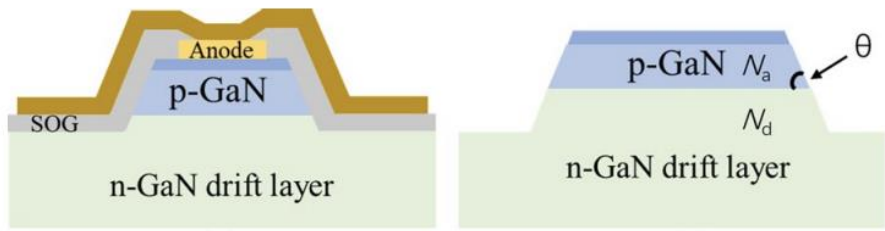
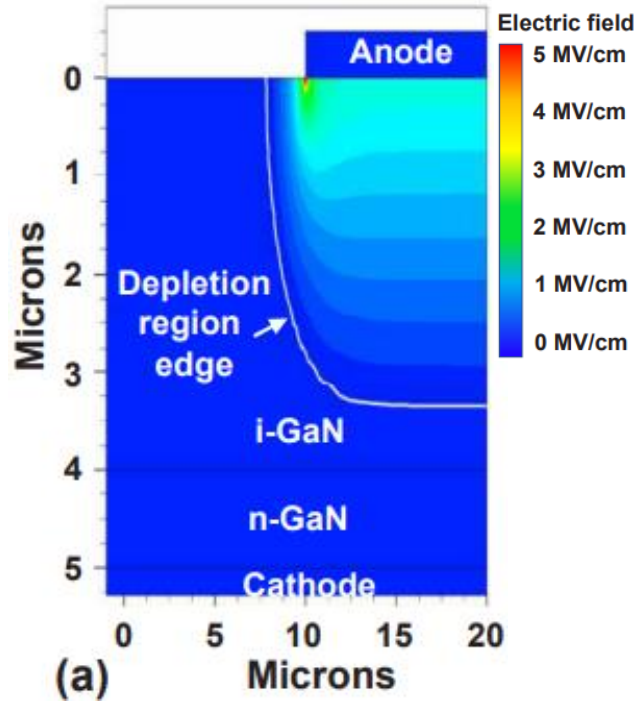


- Drift region:
 - $N_D \approx 5 \times 10^{15} \text{ cm}^{-3}$
 - **drift layer thicknesses are $> 30\mu\text{m}$.**
- Specific on-resistance of 2.95 mohm -cm²
- Breakdown voltages of 3.7 kV



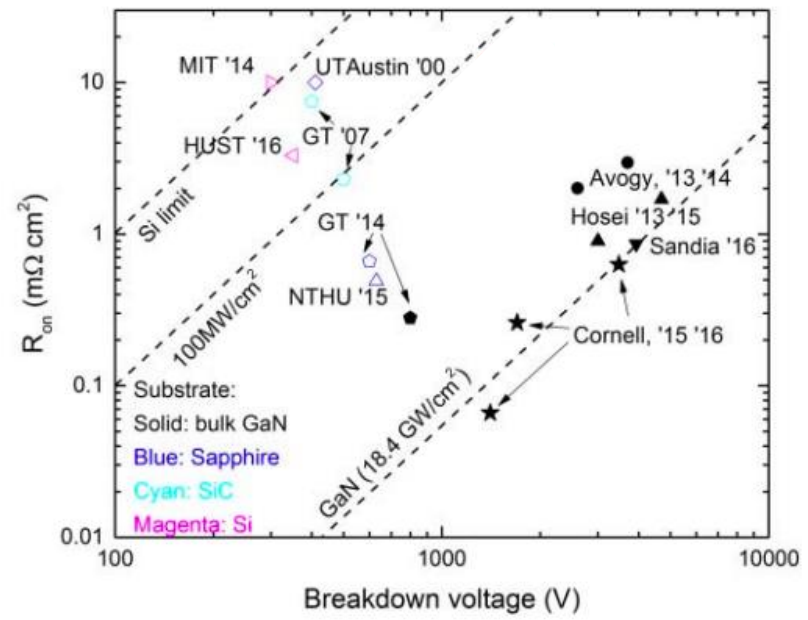
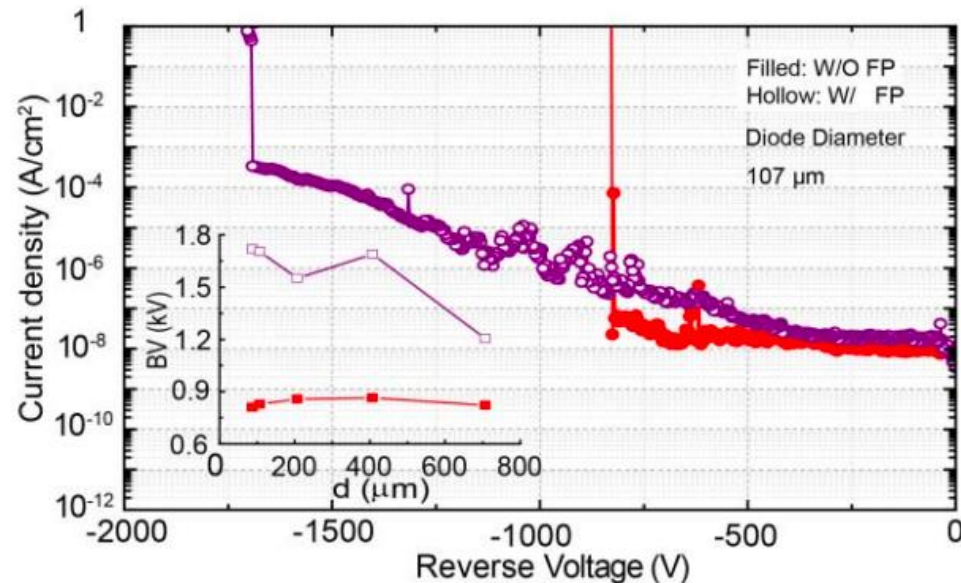
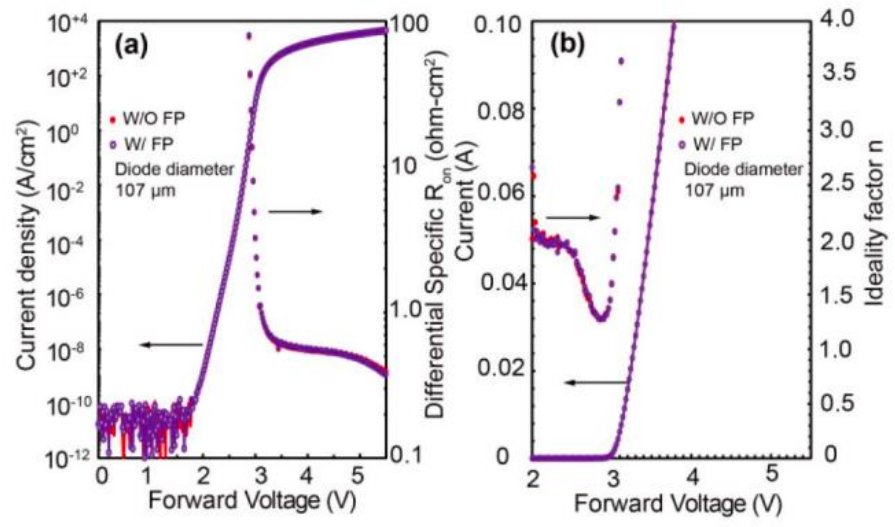
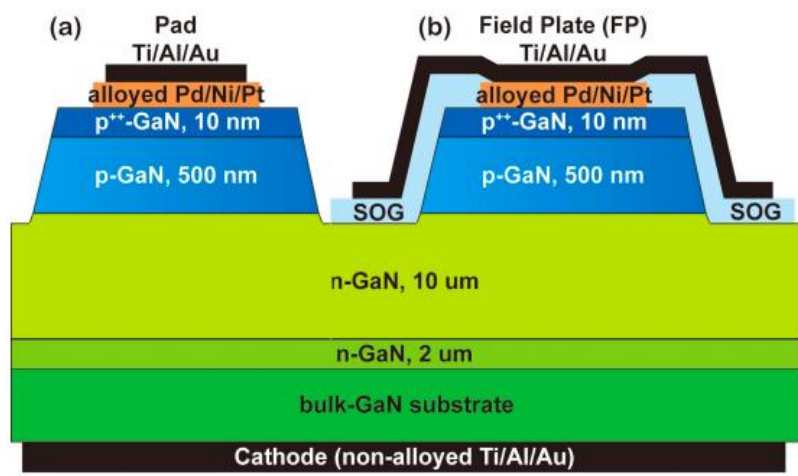
Field plates

High E at Schottky interface
High reverse leakage current

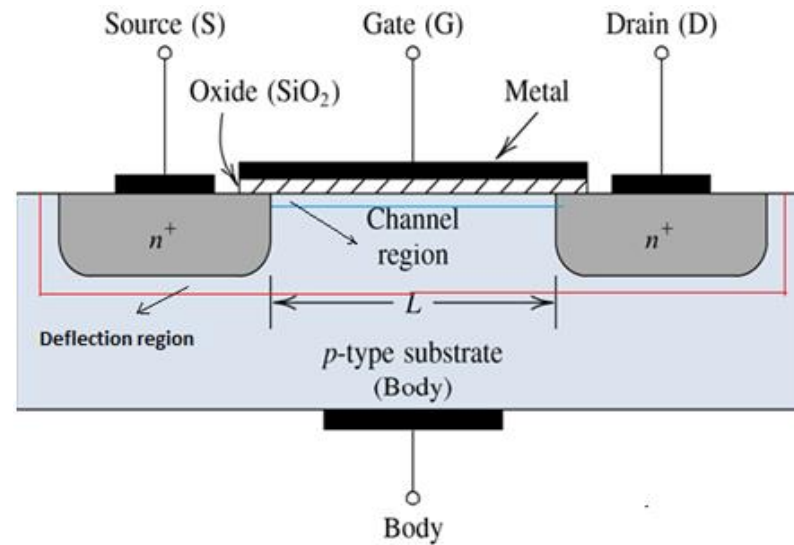


GaN Power PiN diodes

PiN diodes on bulk GaN (10 μm drift layer)



MOSFETs

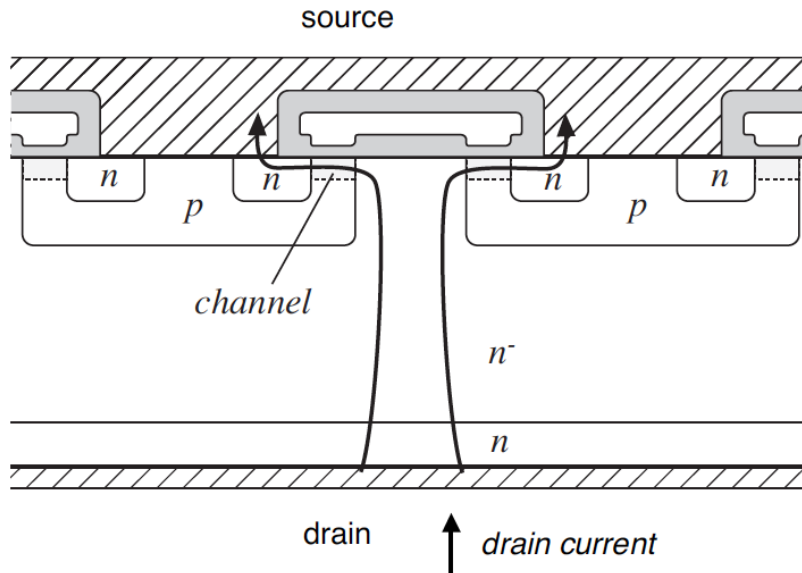


How to make vertical MOSFET?

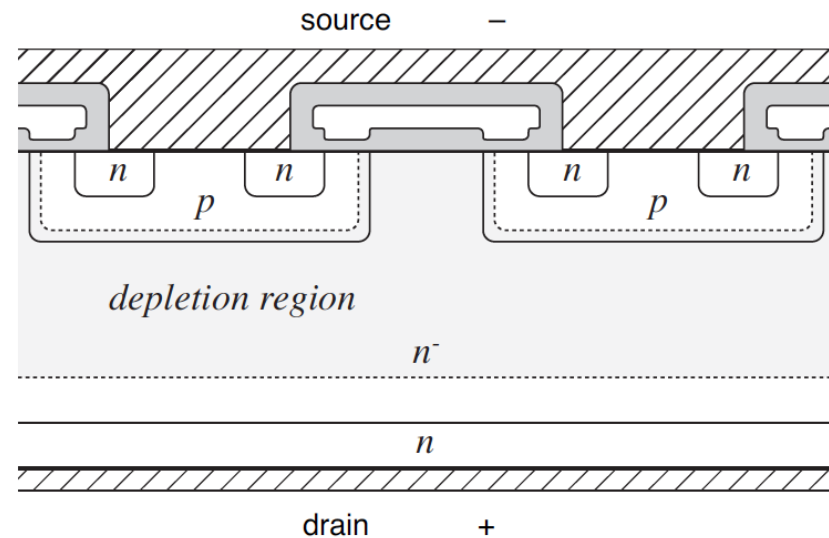
Power MOSFETs

Case of Silicon

Forward polarization: $V_{gs} > 0$



Reverse polarization: $V_{gs} < 0$



There are no minority carriers to cause conductivity modulation:

MOSFETs are majority carrier devices

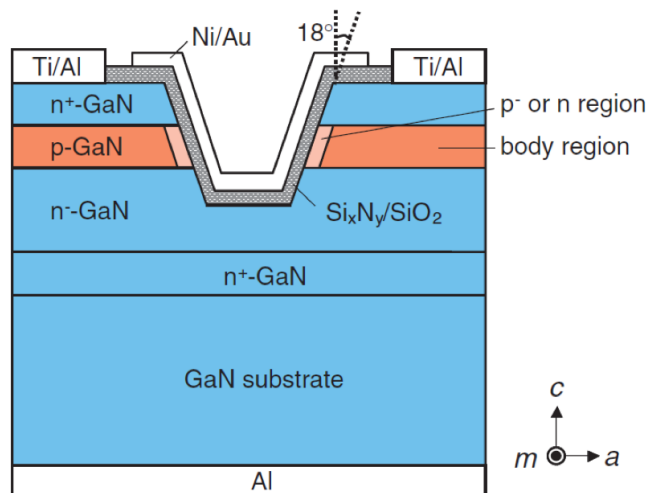
- Breakdown voltage is increased
- On-resistance dominated by resistance of n^- region (drift region)

Reverse polarization:

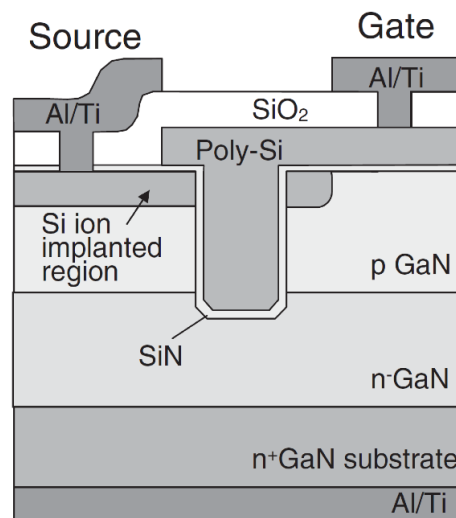
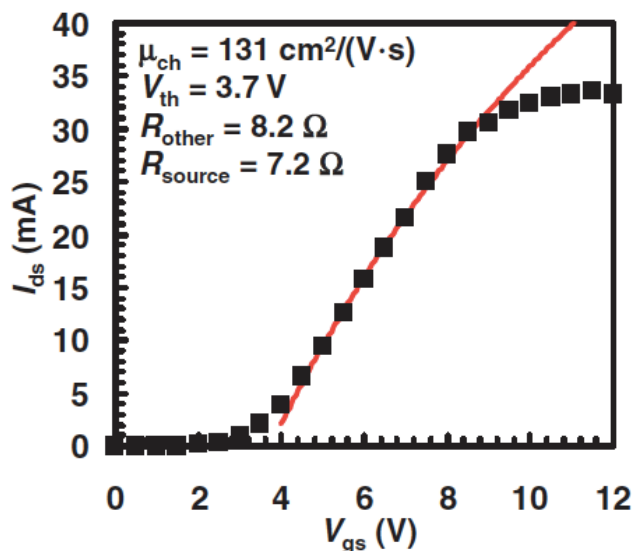
p-n and p- n^- reverse-biased:
voltage drops across n^- region

GaN vertical transistors

Trenched MOSFETs (6 μm -thick n^- -GaN)

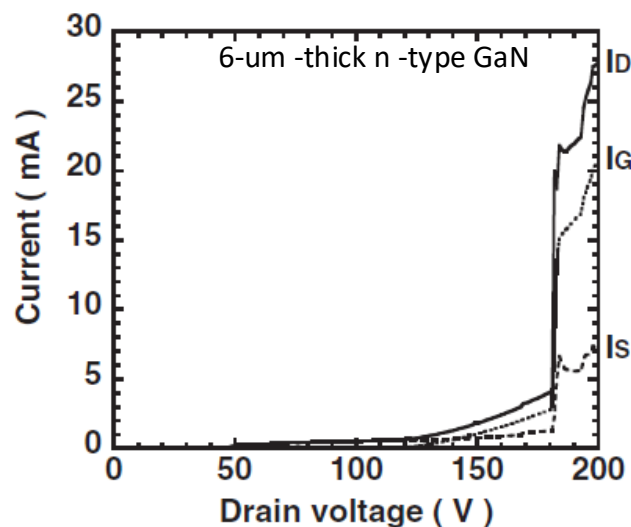


$R_{on} = 9.3 \text{ m}\Omega\cdot\text{cm}^2$
channel mobility: $131 \text{ cm}^2/(\text{Vs})$



Drain

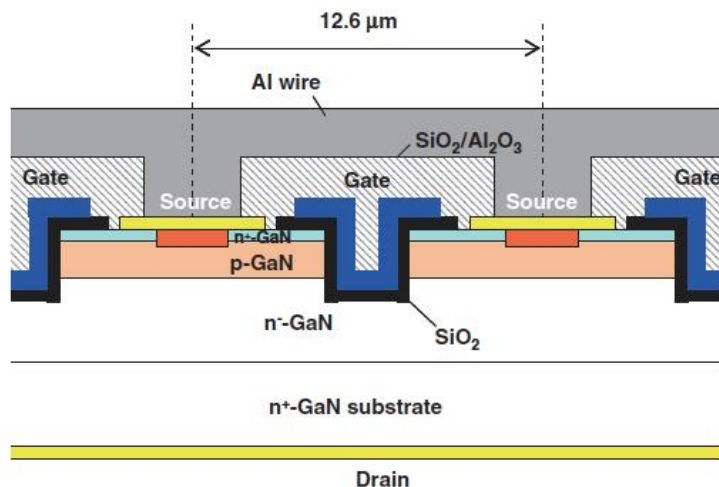
Wet-etch (TMAH) to yield vertical sidewalls



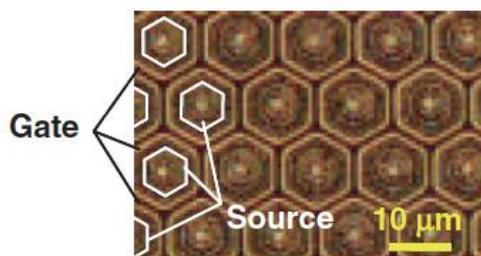
Key challenges:
Large on-resistance
Poor breakdown voltage

GaN vertical transistors

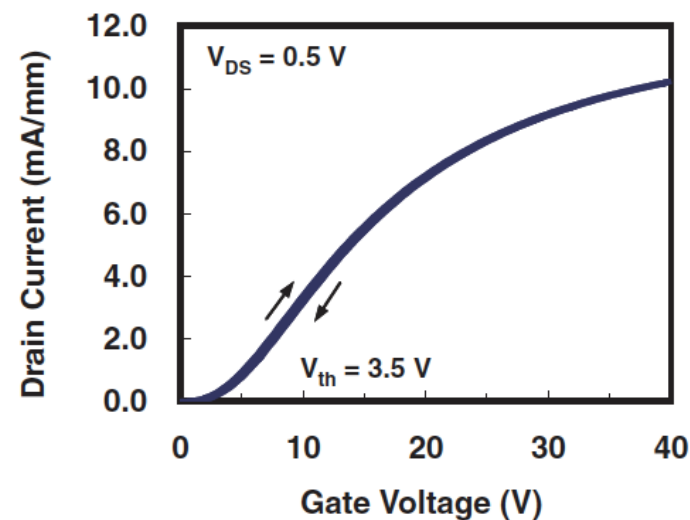
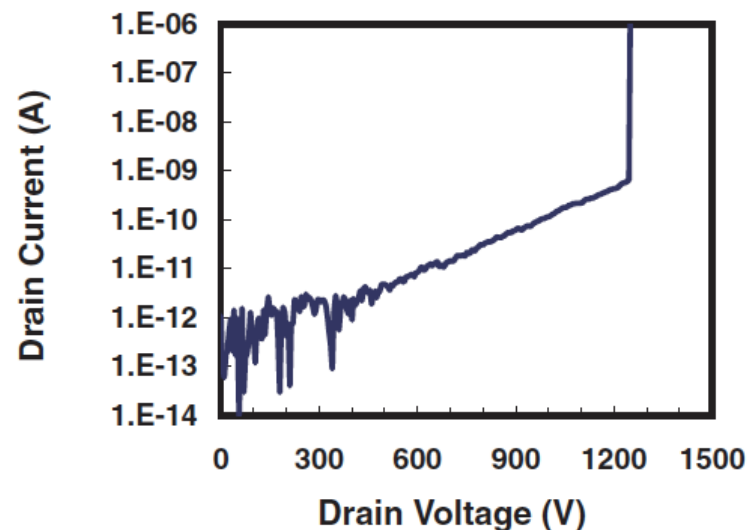
Trenched MOSFETs (13 μm -thick n^- -GaN)



(a)

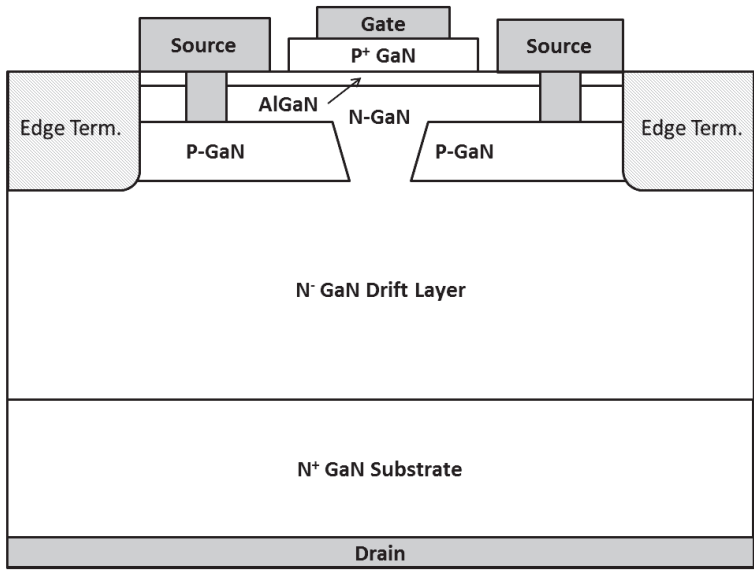


- Specific on-resistance of $1.8\text{m}\Omega \cdot \text{cm}^2$
- 1.2KV breakdown voltage
- 13- μm -thick n^- -GaN
- $N_d = 9 \times 10^{15} \text{ cm}^{-3}$



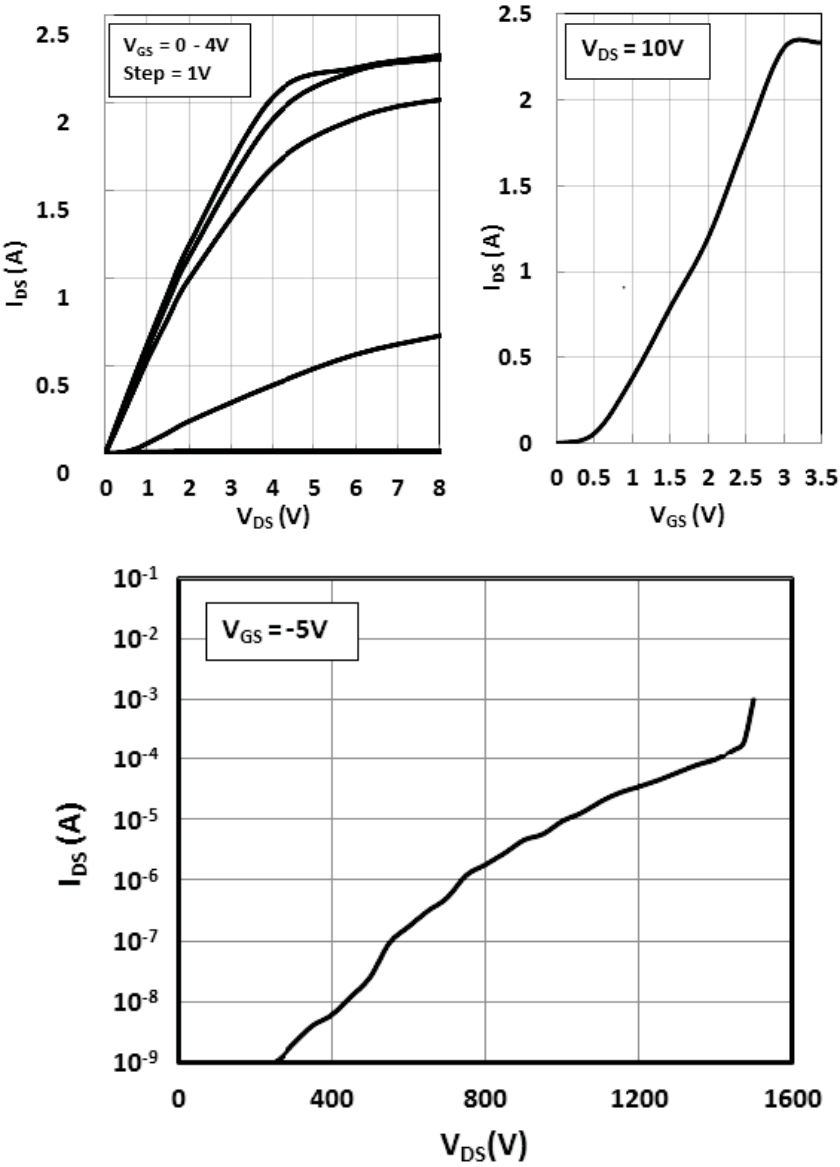
GaN vertical transistors

Vertical devices: CAVETs



drift region net doping: $N_D - N_A = 10^{16} \text{ cm}^{-3}$
drift layer thickness is 15 μm
 $R_{on} = 2.2\text{-m-cm}^2$

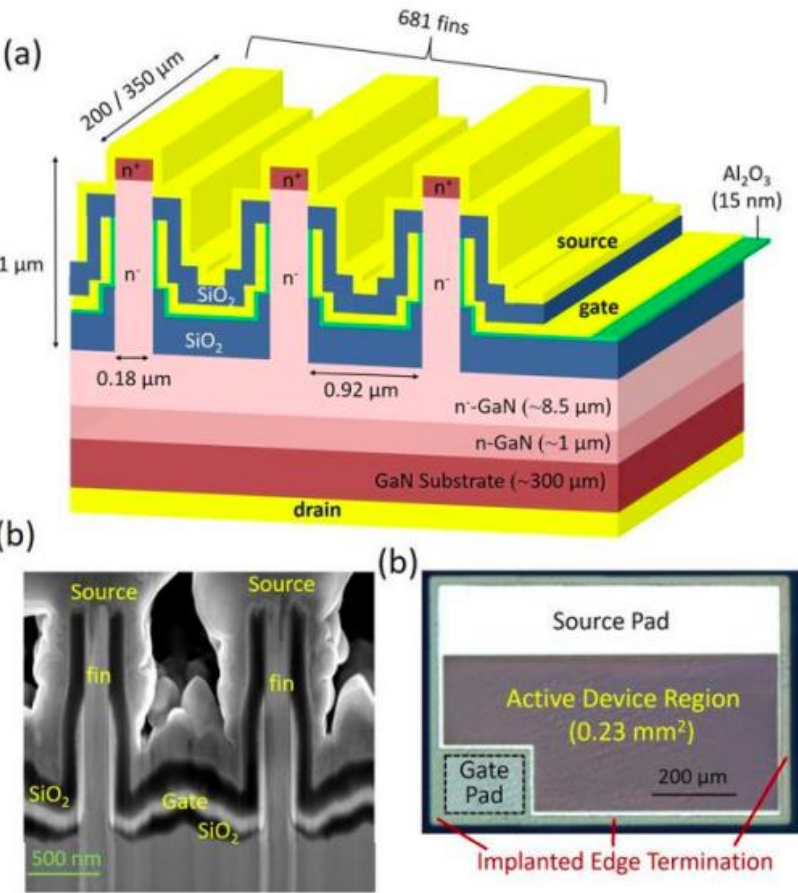
- Doesn't rely on channel on the p-GaN
- Normally-off behavior is difficult



GaN vertical transistors

Vertical devices: Unipolar device

Work function difference between the gate metal and GaN depletes all electrons: enables normally-off operation.



fin width: 180 nm

threshold voltage of 1.3 V

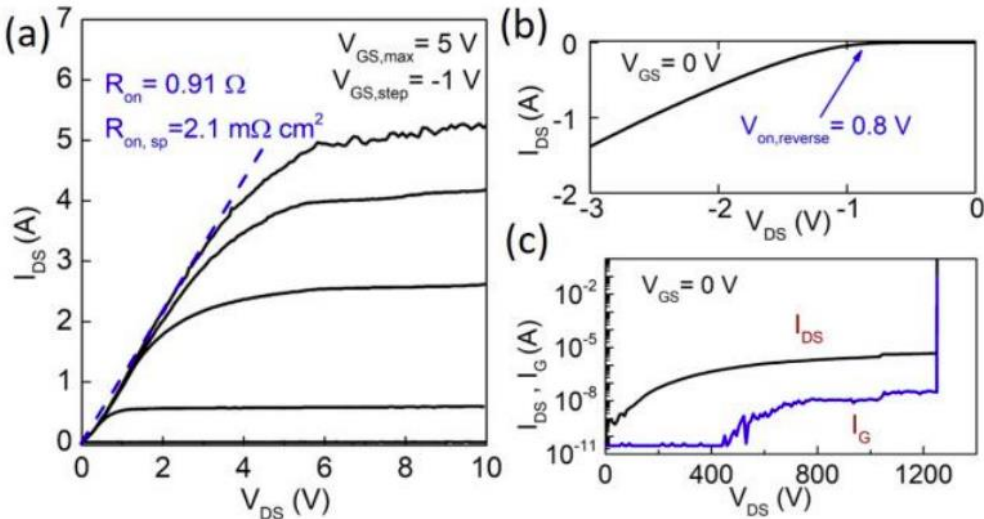
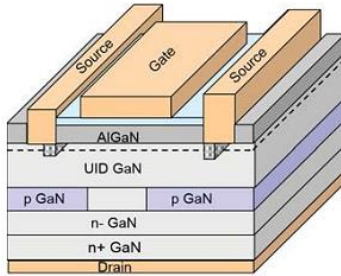


Fig. 2. (a) Device output curves and the extracted R_{on} and $R_{sp,on}$. (b) Reverse conduction curves and the extracted reverse turn-on voltage. (d) Off-state leakage characteristics at $V_{GS}=0$ V with a BV of 1250 V.

Vertical GaN devices on Silicon substrate

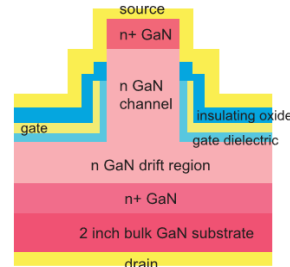
There has been a significant progress on GaN vertical devices on bulk GaN substrates:

CAVET



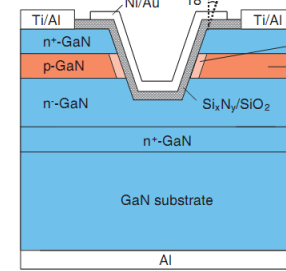
UCSB, Avogy, Toyoda, UC Davis

Fin MOSFET



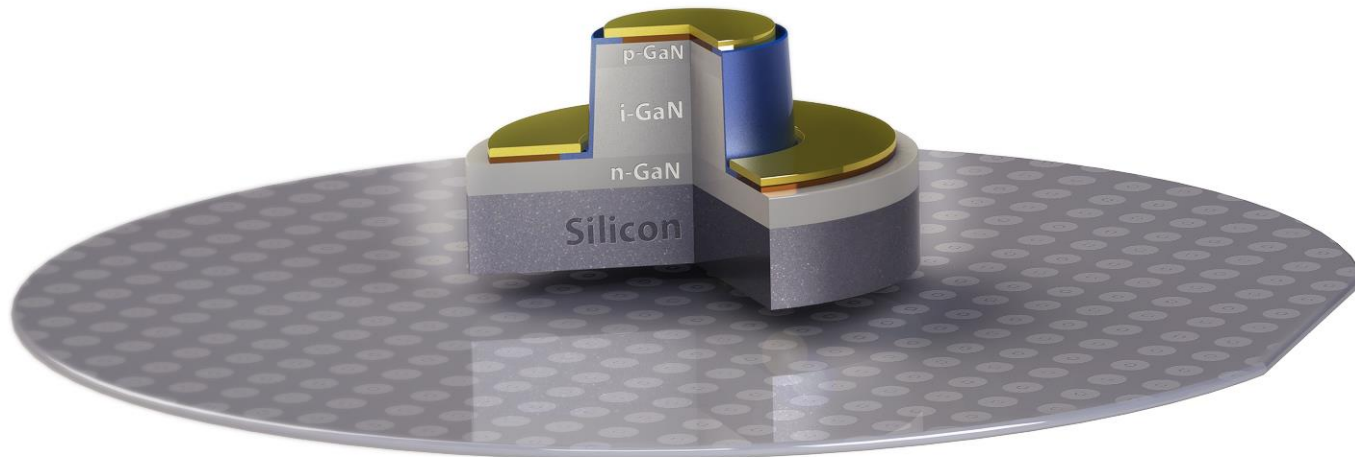
MIT

Trench MOSFET



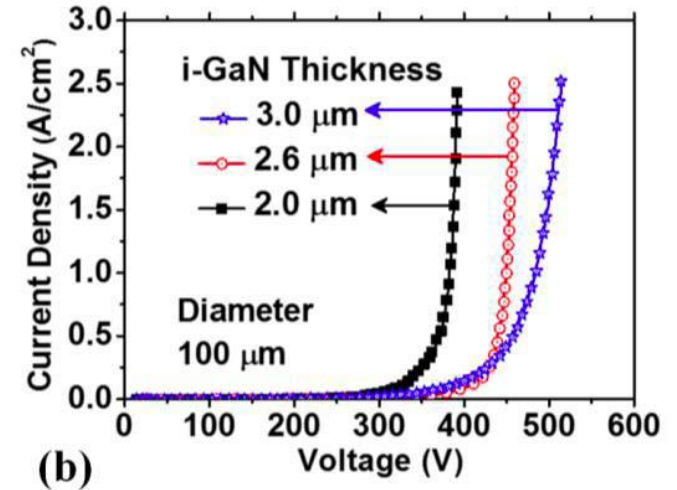
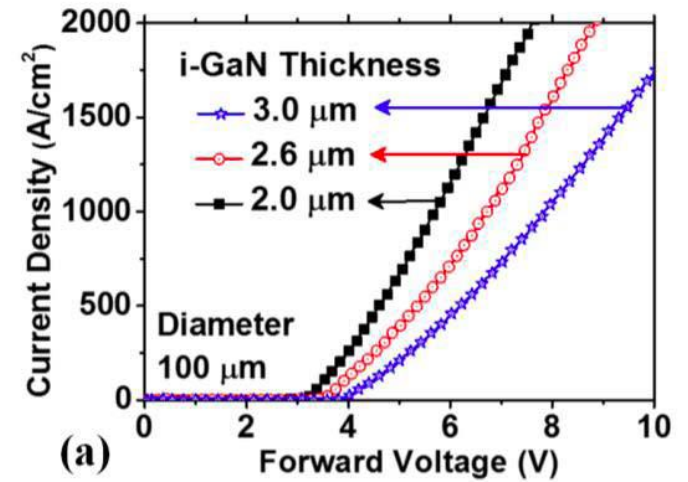
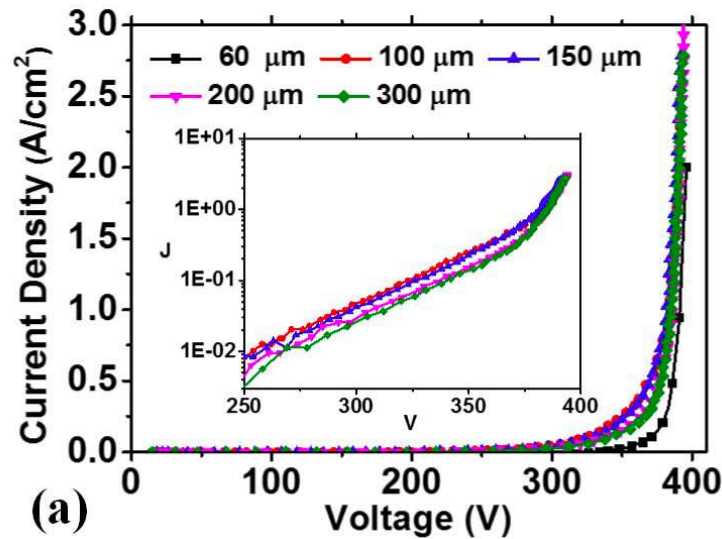
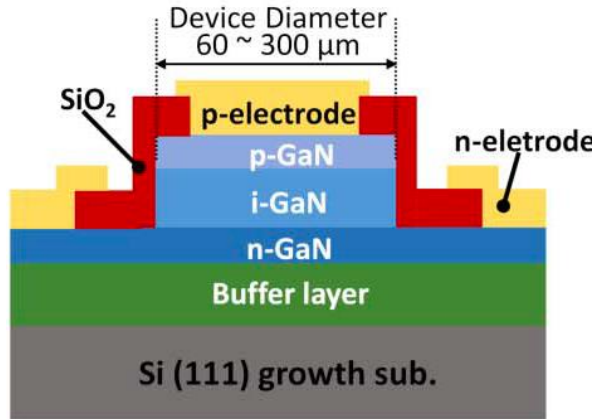
UCSB, Toyoda, ROHM

Our approach: Vertical GaN-on-Silicon devices



GaN Power PiN diodes

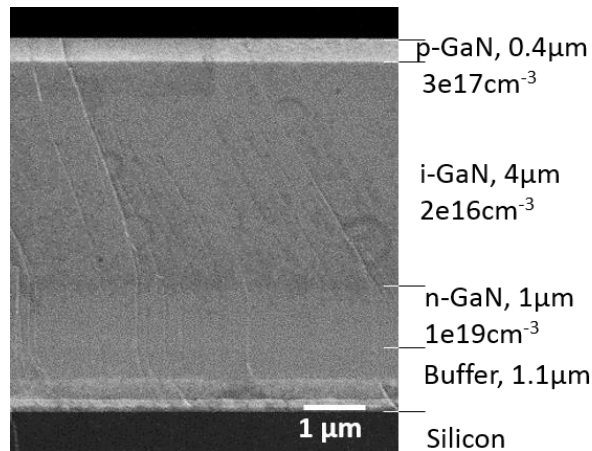
GaN PIN diodes on Silicon substrates (< 3μm drift layer)



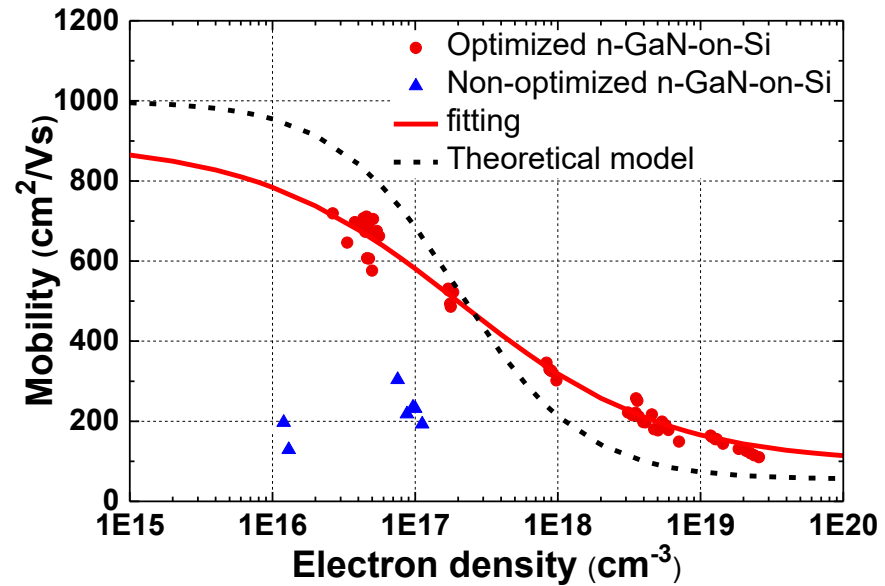
- 2-μm-thick undoped i-GaN layer
- specific on-resistance of 2.6 mohm –cm²
- breakdown voltages of 390 V

First Challenge: growth of thick GaN on Si

6.5 μm -thick GaN grown on 6"-silicon substrate



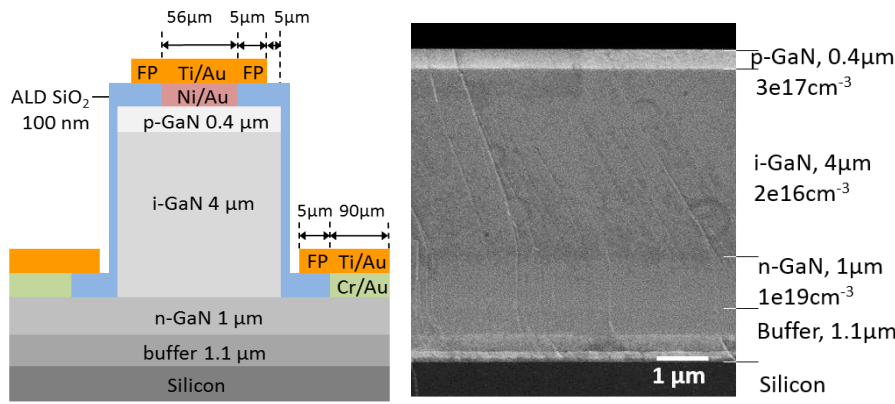
4 μm -thick drift



- FWHM of 235 arcsec and 307 arcsec in (002) and (102) directions
- Estimated TDD of $2.95 \times 10^8 \text{ cm}^{-2}$
- Excellent mobility of 720 cm^2/Vs in UID-GaN

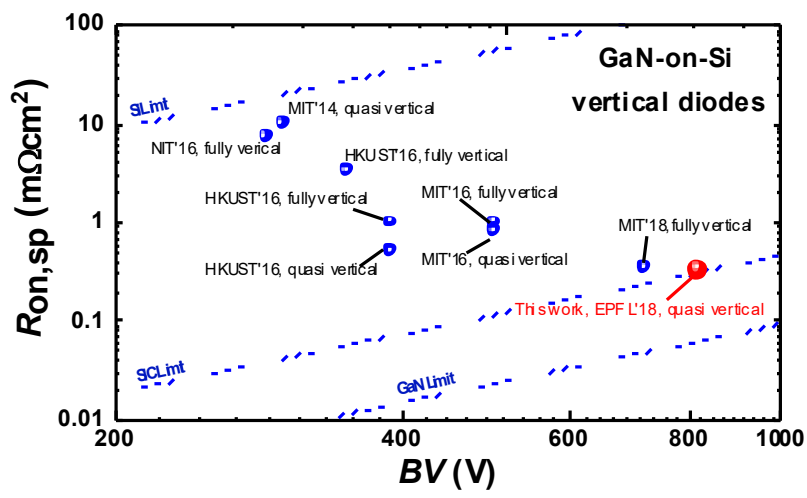
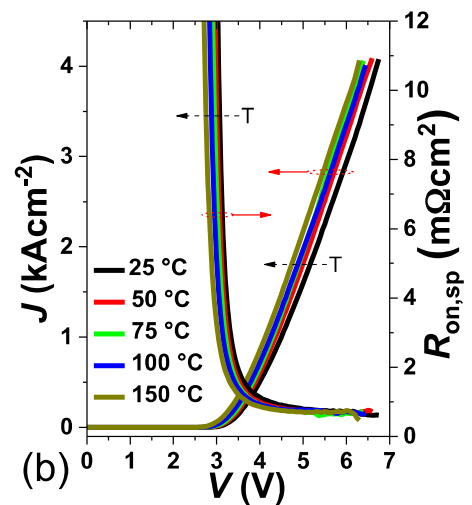
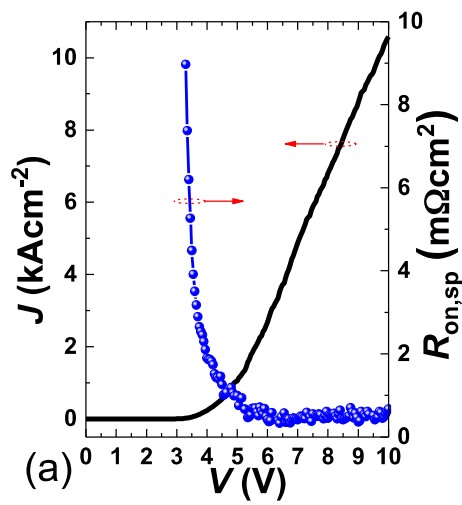
Epi structure by Dr. Kai Cheng,
Enkris semiconductors

Quasi-vertical GaN-on-Si power devices



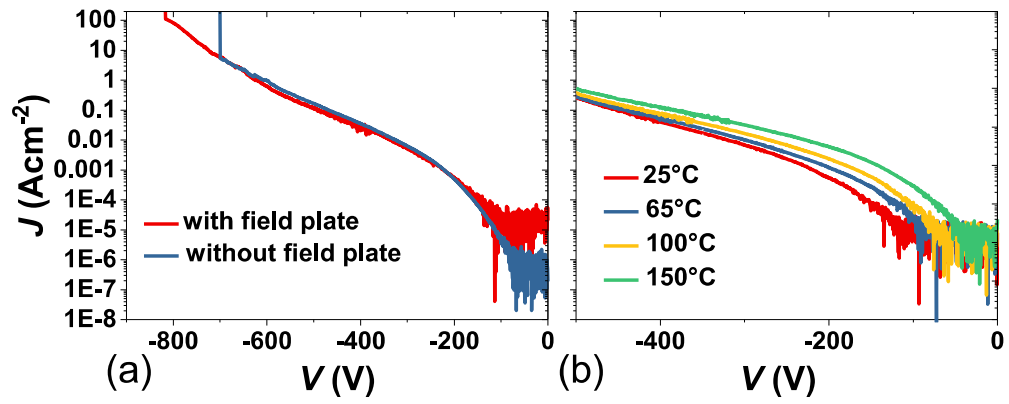
Current density over 13 kA/cm²
Low RON 0.3 mΩcm²

Excellent mobility of 720 cm²/Vs in UID-GaN,



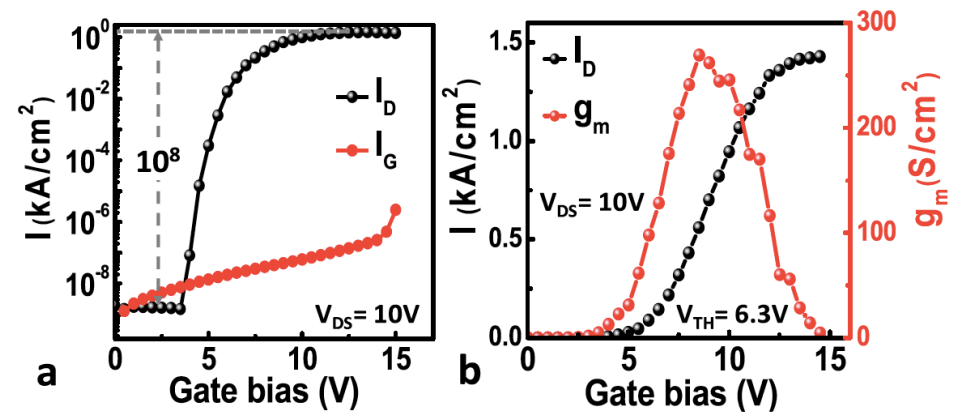
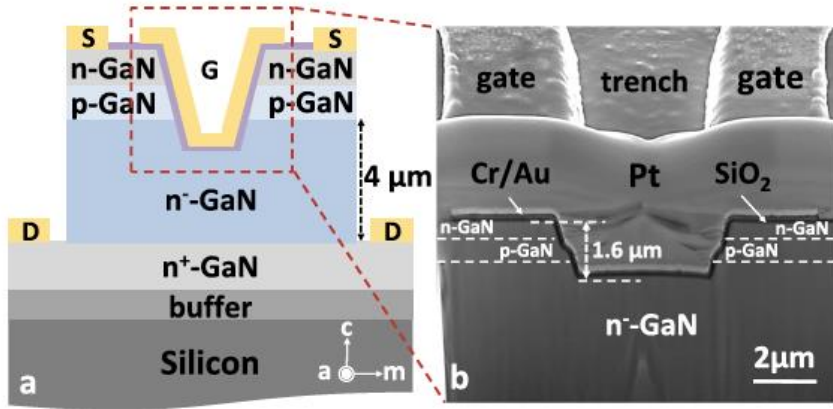
Excellent performance with a BFOM of 2.0 GW/cm²

High breakdown voltage of 820 V

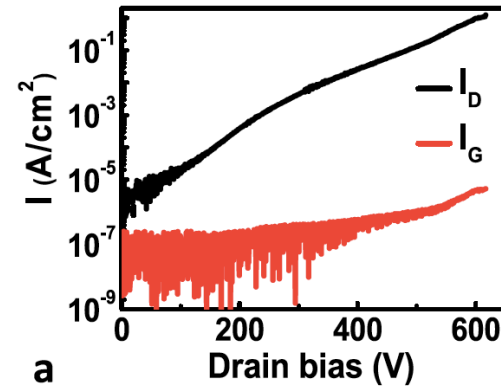
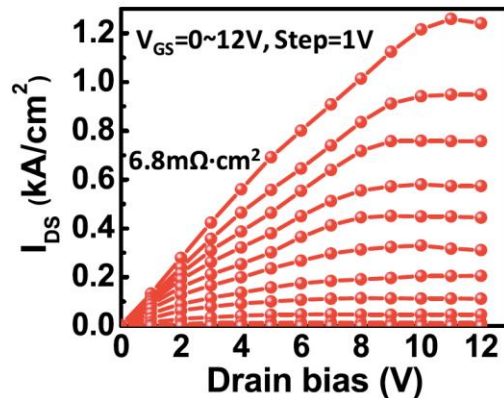


Quasi-vertical power devices

How about vertical GaN power transistors on cost-effective Silicon substrates:



High breakdown voltage of 645 V

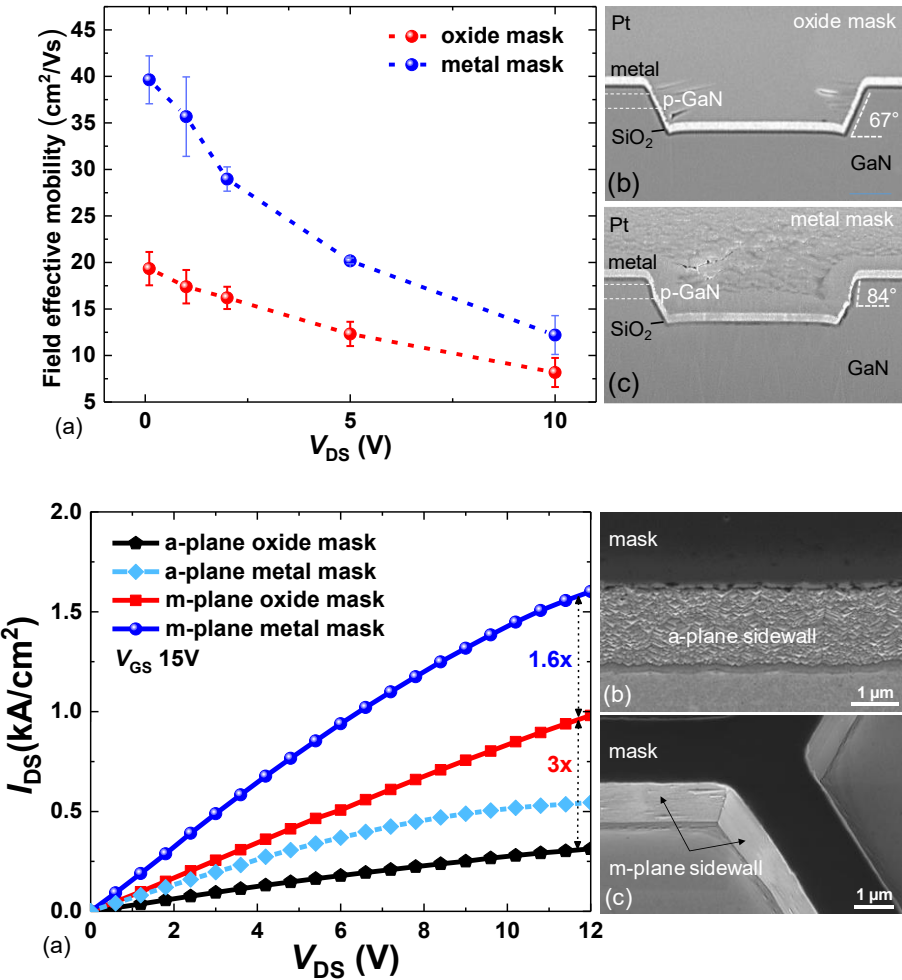
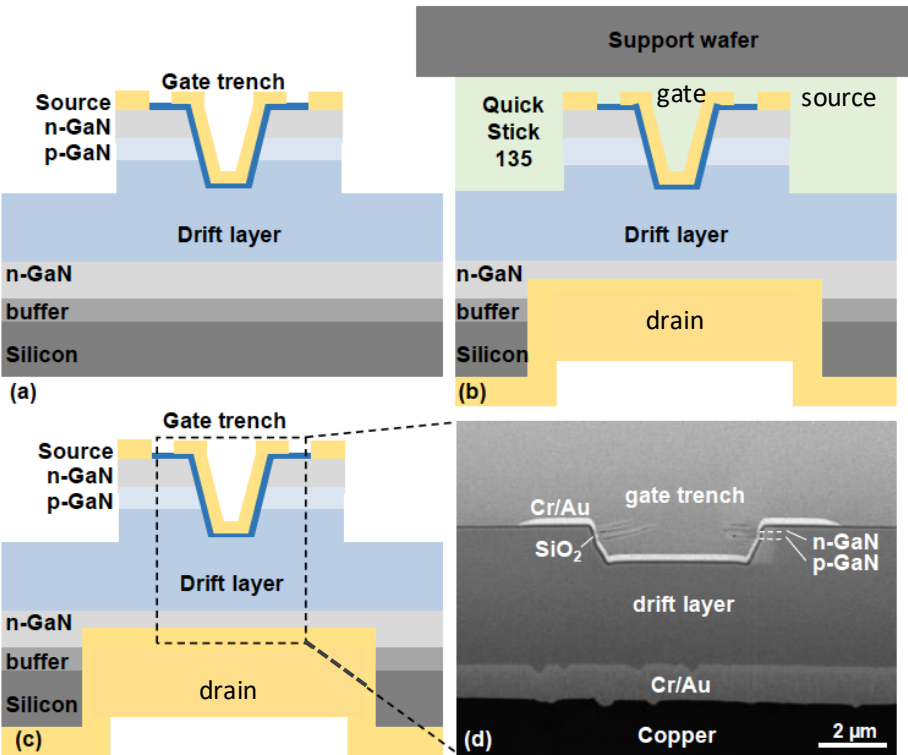


Large on-resistance:

- Poor channel mobility of 17.8 cm²/V.s
- Quasi-vertical: current crowding at n-GaN layer

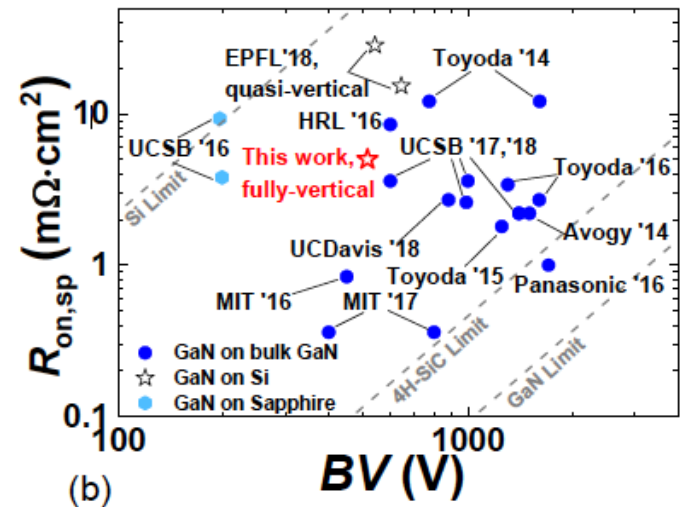
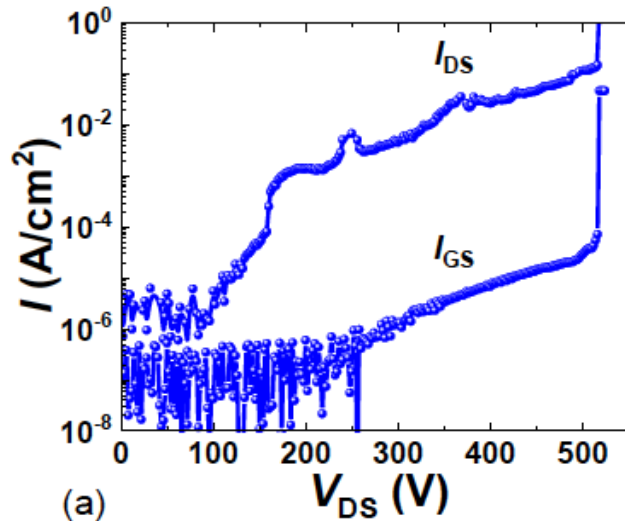
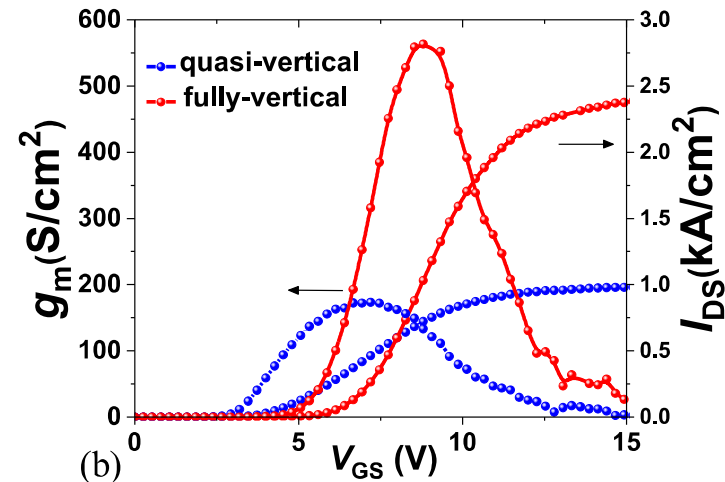
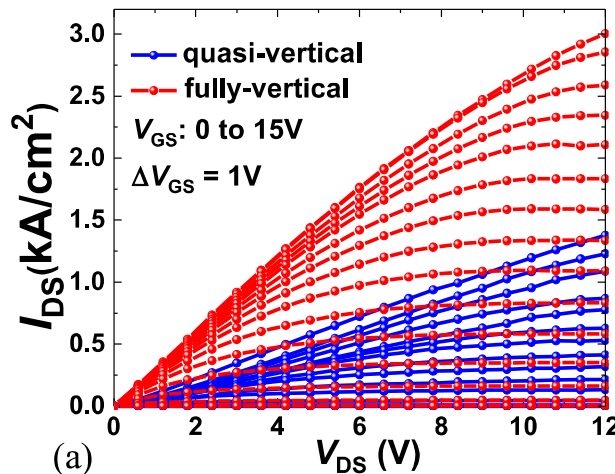
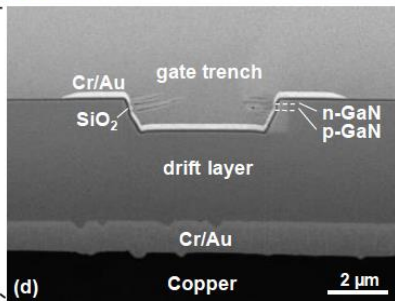
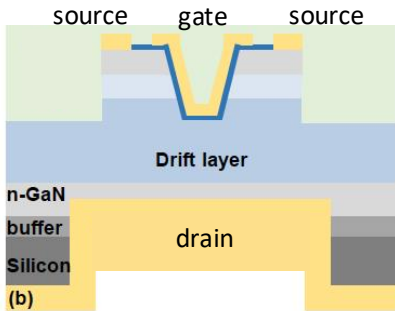
First fully-vertical power transistors on Silicon

Demonstration of fully vertical GaN power transistors on cost-effective 6" Silicon



Fully-Vertical power transistors

First demonstration of fully vertical GaN power transistors on cost-effective Silicon



Major step toward high-performance GaN vertical power transistors on low-cost silicon substrates

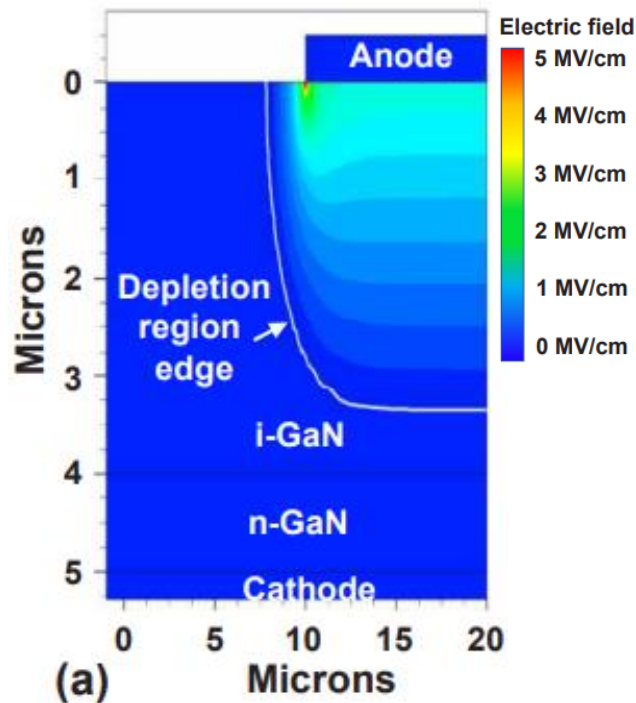
Advanced concept:

Field management using polarization engineering

Can we use a low band-gap material for higher voltage devices?

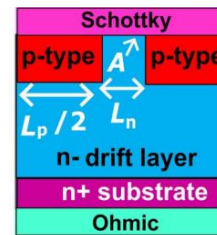
Schottky Barrier Diode (SBD)

High E at Schottky interface
High reverse leakage current

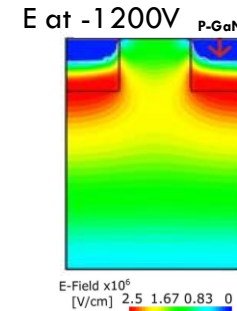


R. A. Khadar *et al.*, ISPSD, pp. 147-150 (2021)

Junction Barrier Schottky (JBS)

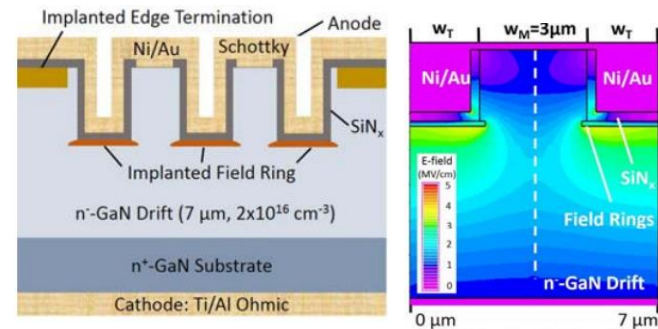


Inevitable R_{on} increase



M. Matys *et al.*, Jpn. J. Appl. Phys. 62, SN0801 (2023)

Trench MOS Barrier Schottky (TMBS)



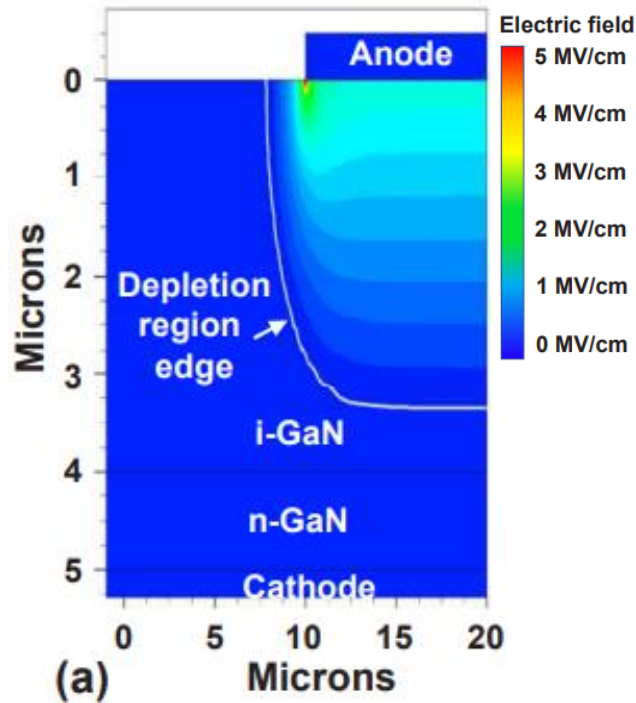
Careful design/complex fabrication process

Y. Zhang *et al.*, IEDM, pp. 10.2.1-10.2.4 (2016)

Schottky Barrier Diode (SBD)

High E at Schottky interface

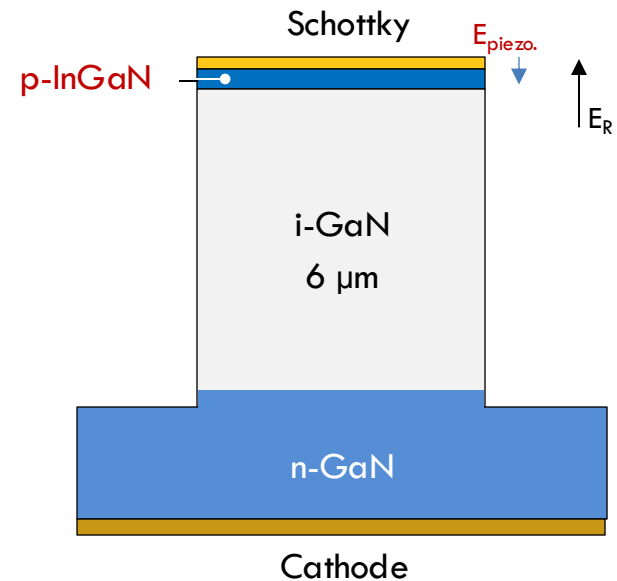
High reverse leakage current



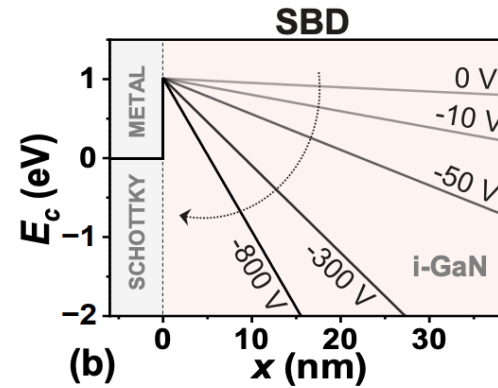
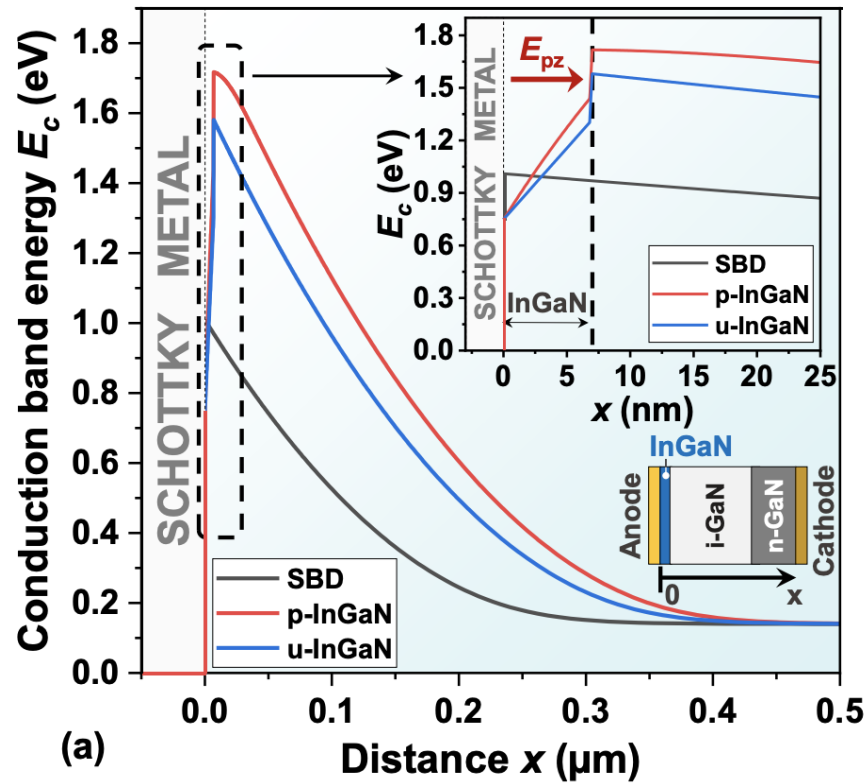
R. A. Khadar *et al.*, ISPSD, pp. 147-150 (2021)

Our approach:

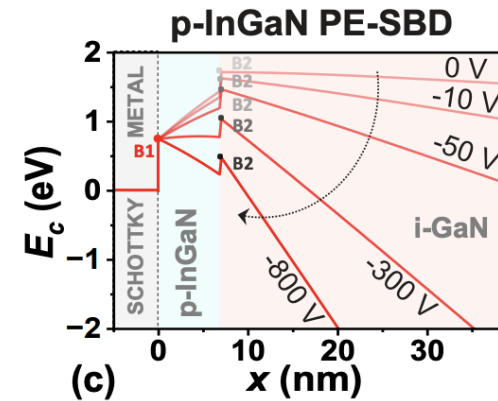
Polarization fields of InGaN for field management



Can we use a low band-gap material for higher voltage devices?

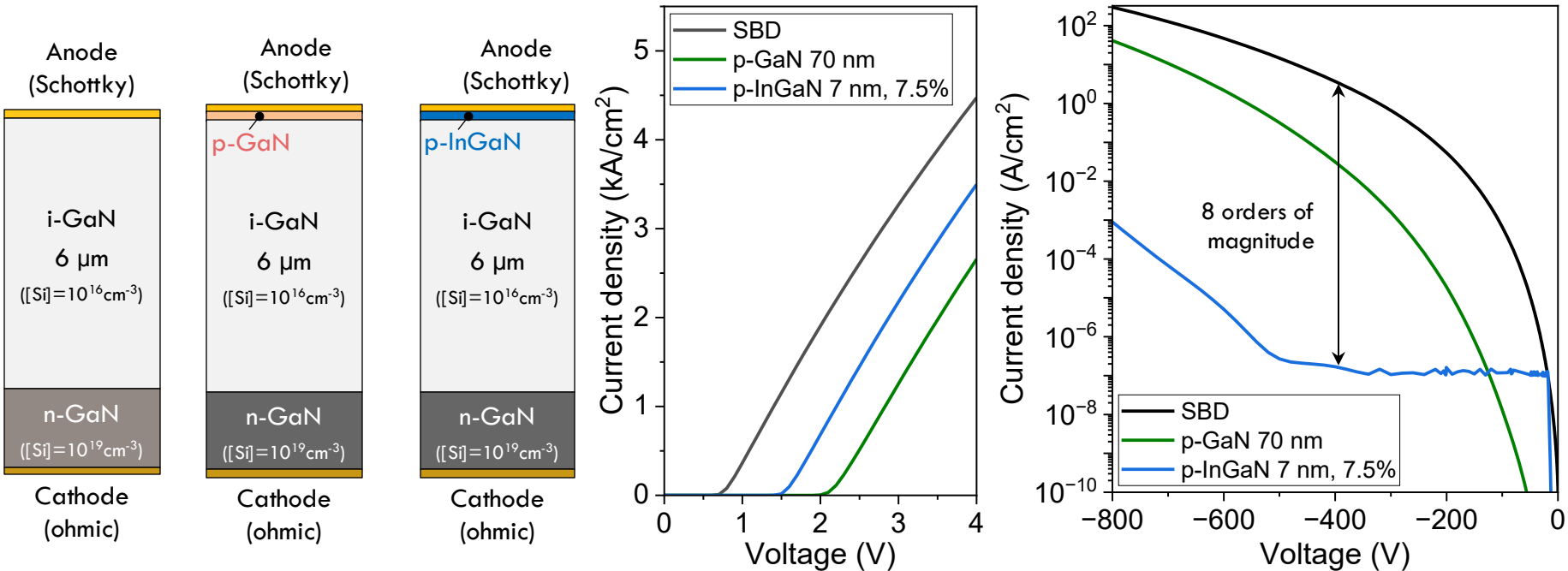


At -800 V:
 $E_{\text{max}} = 1.94 \text{ MV/cm}$



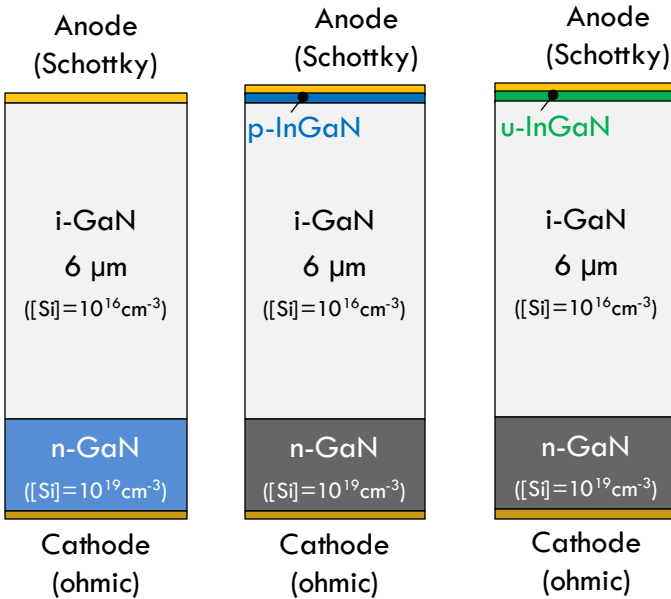
At -800 V:
 $E_{\text{max, p-InGaN}} = 0.9 \text{ MV/cm}$

Piezoelectric field (+) in p-InGaN opposes external reverse electric field (-)

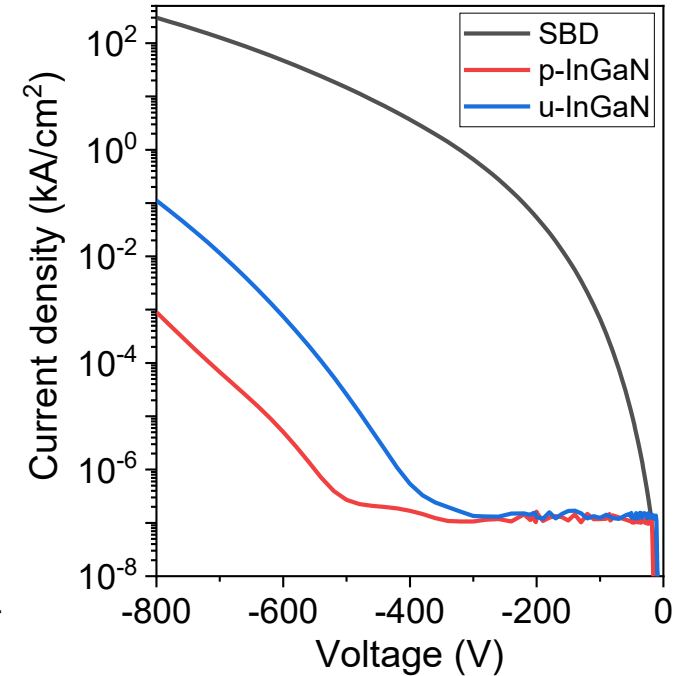
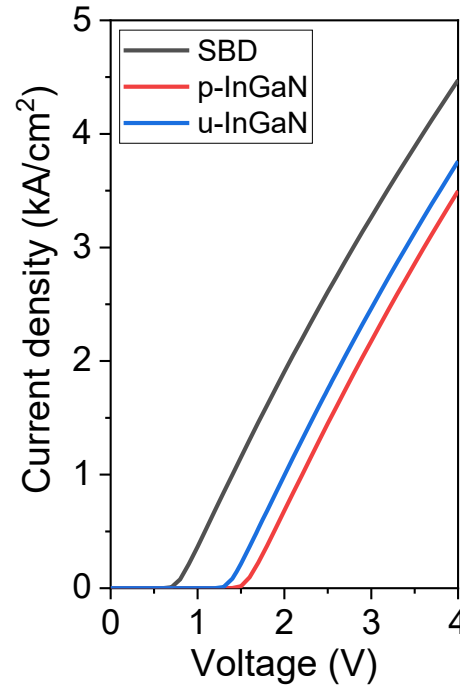


Large decrease in leakage current using thin p-InGaN

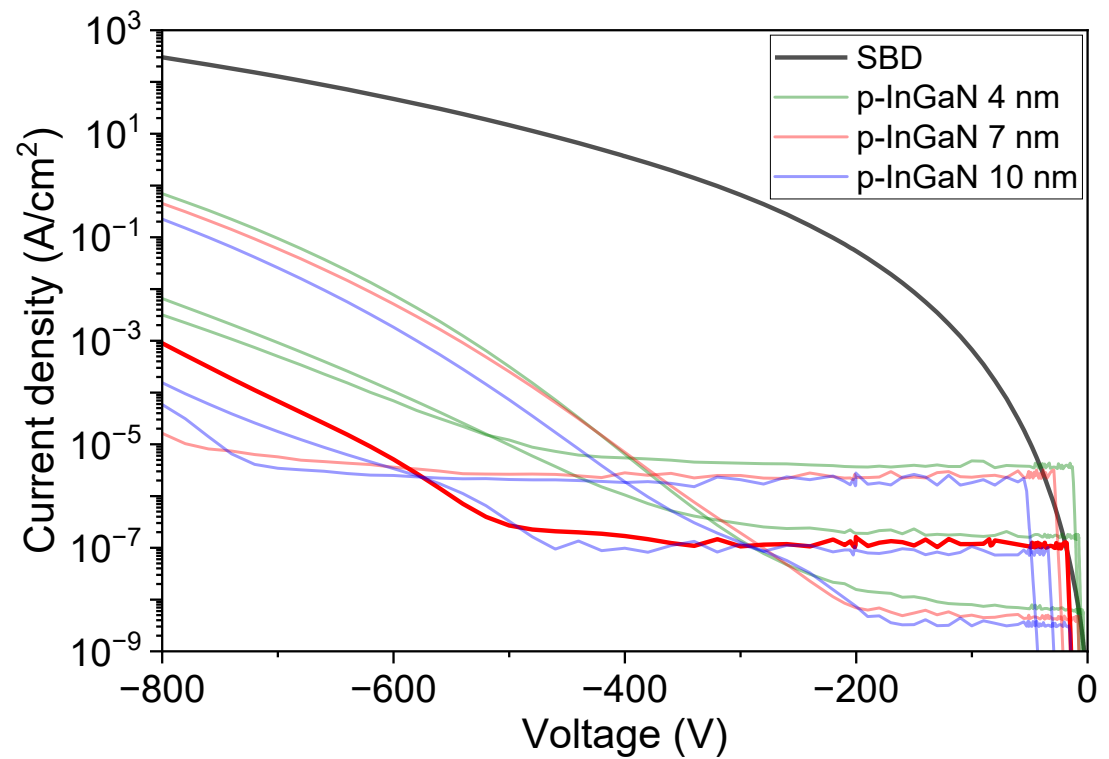
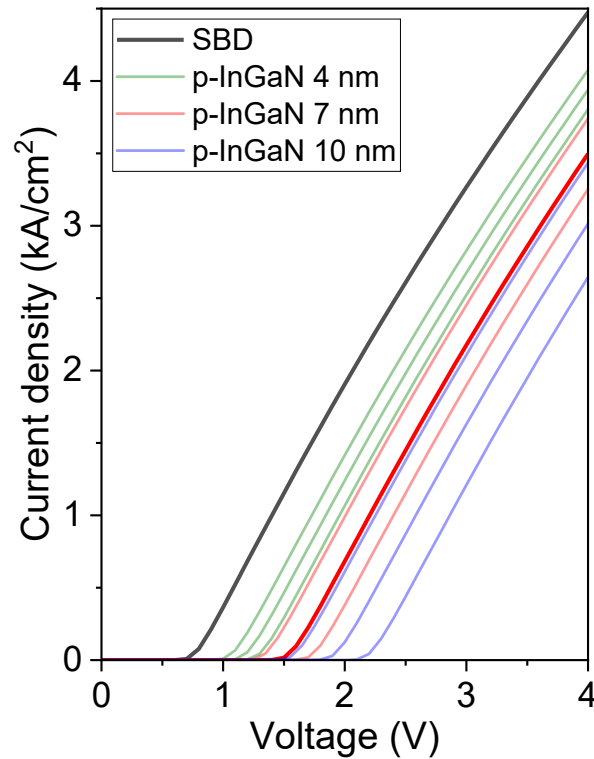
TCAD simulations: p-InGaN vs. uid-InGaN



InGaN 7 nm, [In] = 7.5%

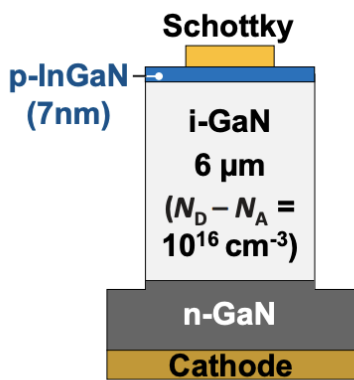


Piezoelectric polarization of InGaN:
Dominant contribution to electrical performances

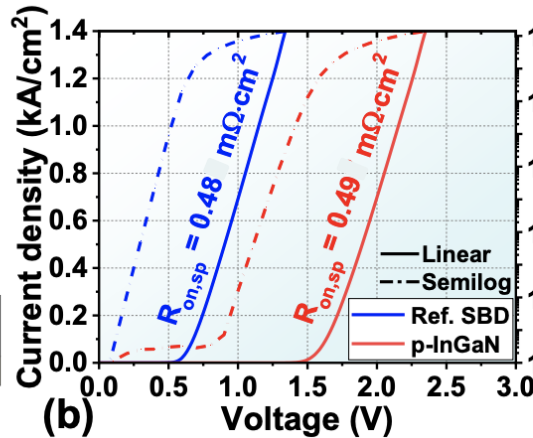


A thickness of 7 nm and $[\text{In}] = 7.5\%$ offer the best compromise

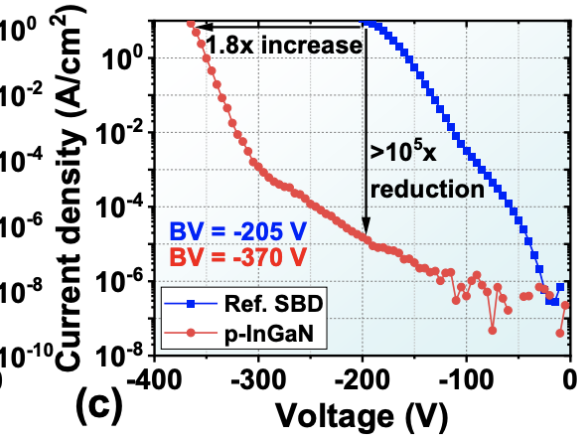
p-InGaN/GaN SBDs with High BV with low RON



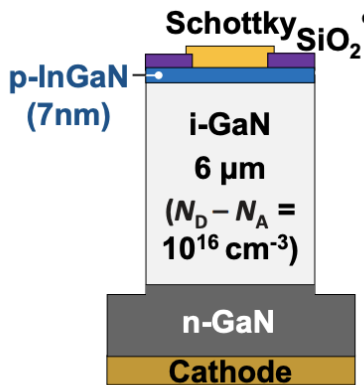
(a)



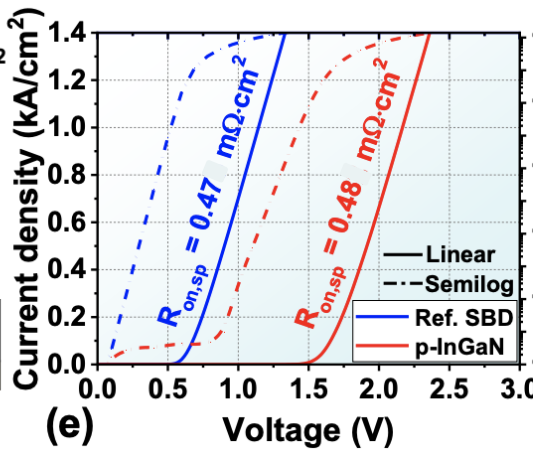
(b)



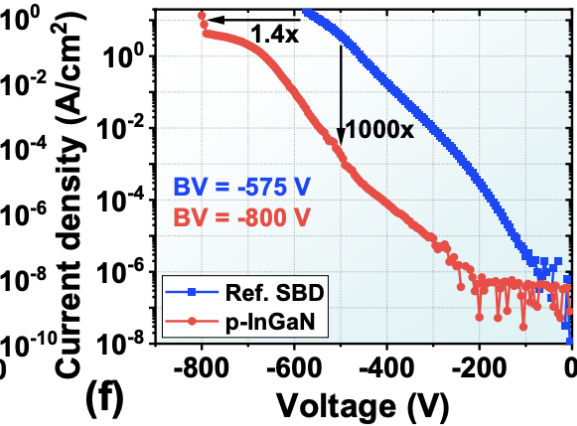
(c)



(d)



(e)

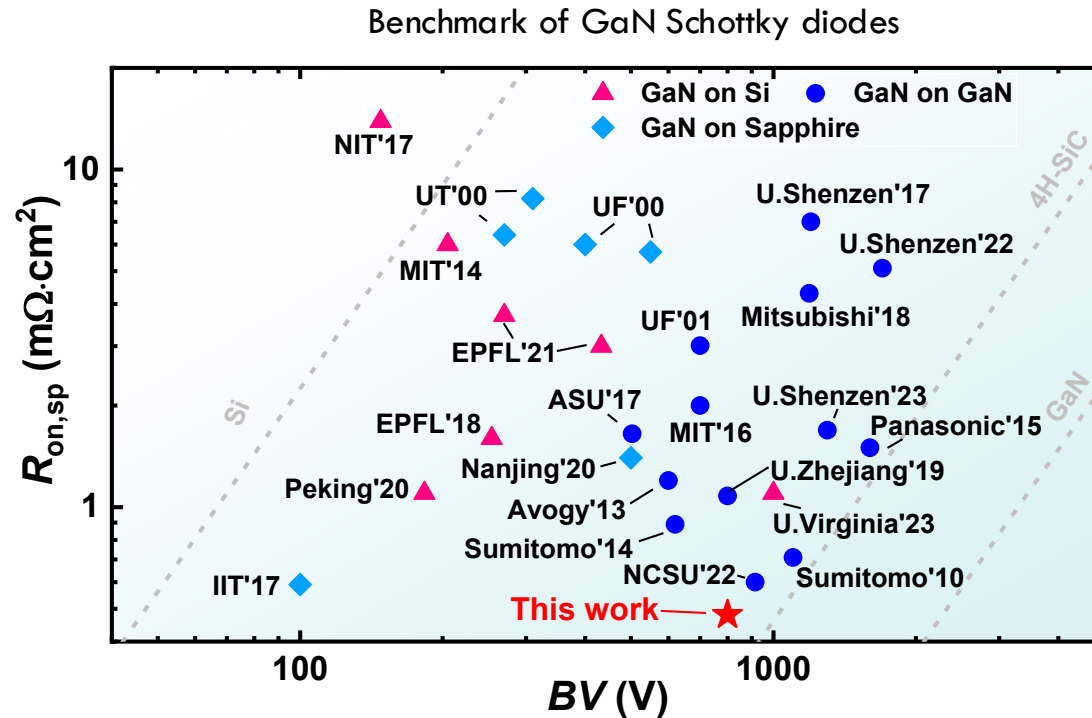


(f)

$R_{\text{ON}}: 0.48 \text{ m}\Omega\cdot\text{cm}^2$
BV: 800 V

Low band-gap InGaN for larger voltage devices

High Baliga Figure-of-Merits (BFOM)



High Baliga Figure-of-Merit (BFOM) = 1.32 GW/cm²

Vertical power devices on bulk GaN:

- Excellent performance near the GaN limits with text-book like features

Future challenges:

- Substrate too expensive and too small
- Localized doping: can we use ion implantation effectively in GaN?
- Improved Mg-doping: low activation of Mg dopants leads to poor transport in the channel

Vertical GaN-on-Si power devices:

- Relatively thick GaN layers on Silicon
- Quasi-vertical PiN diodes and MOSFETs
- First demonstration of fully-vertical GaN-on-Si MOSFET

Future challenges:

- Growth of thicker drift GaN layers
- Reduction of dislocation density

Low band-gap InGaN for larger voltage devices